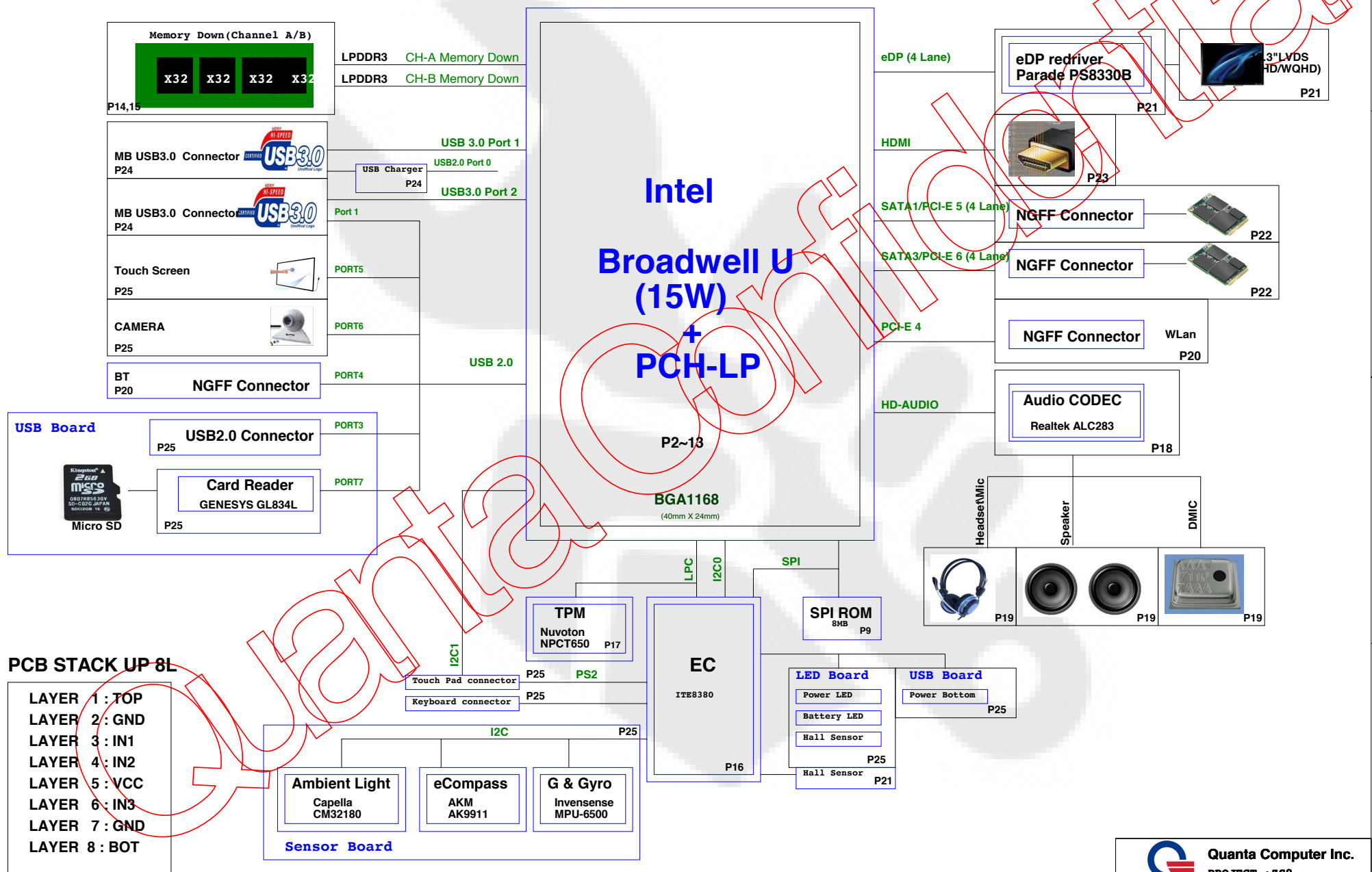
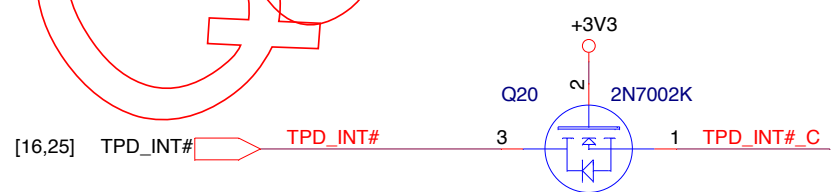
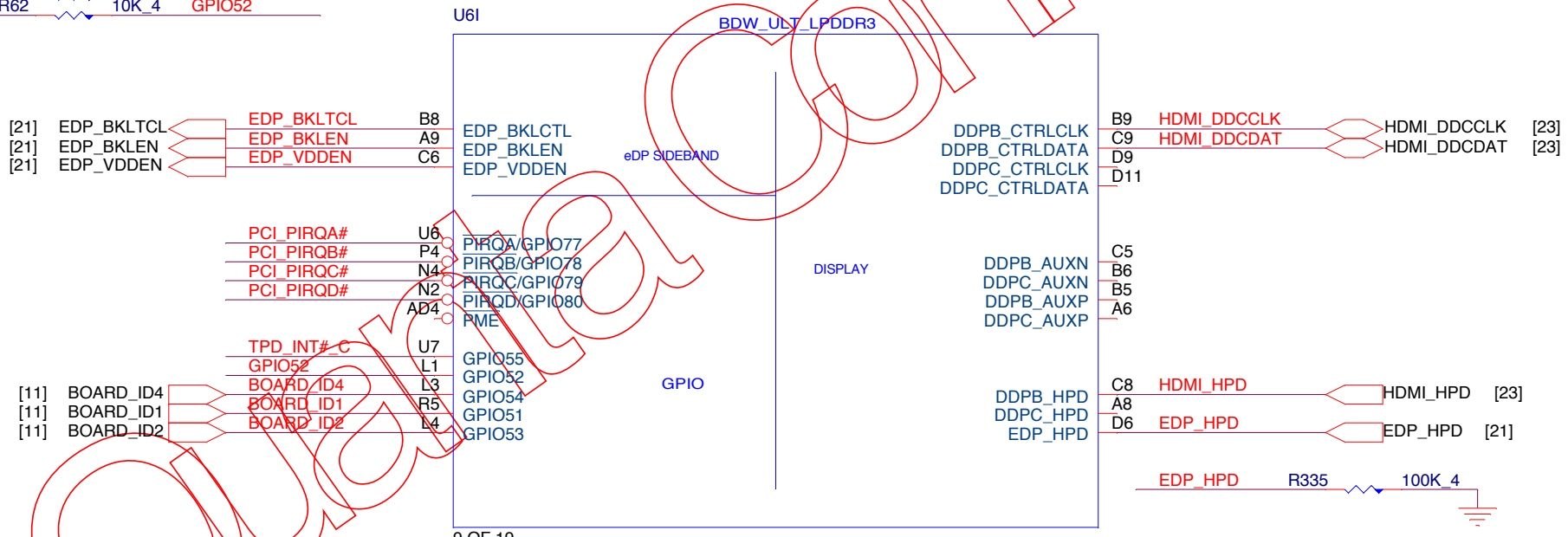
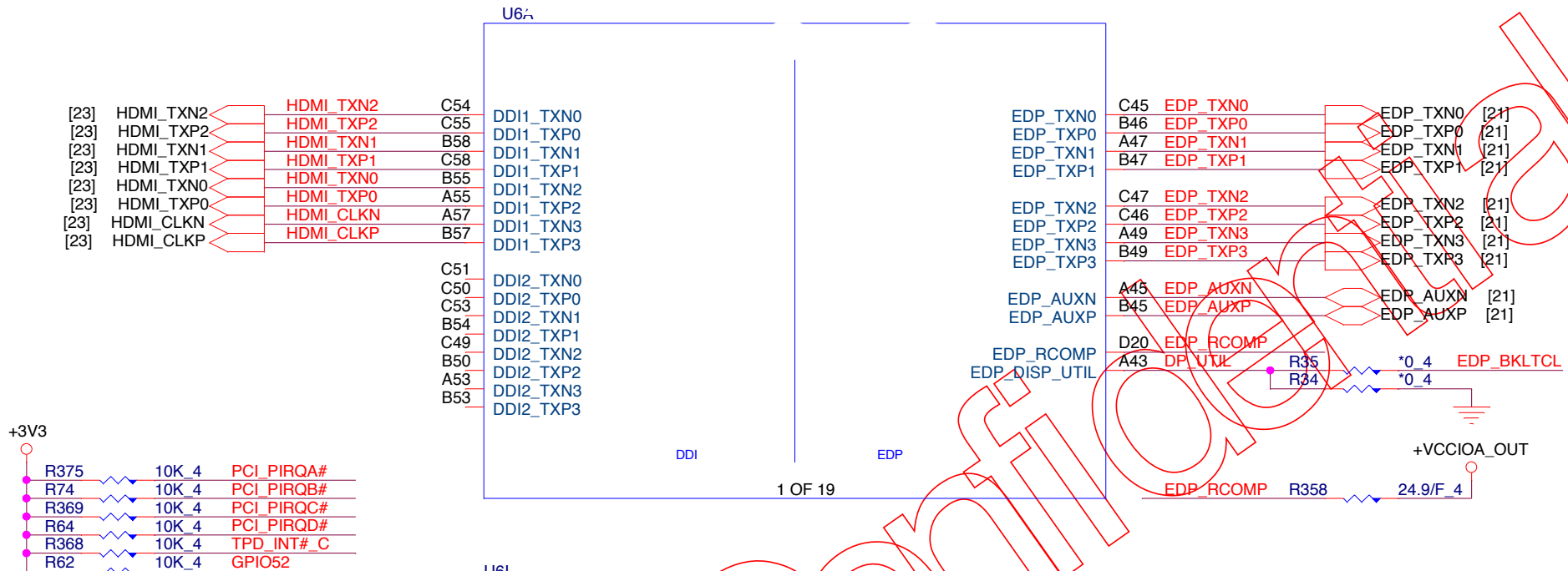



# ZS8 LPDDR3 BDW ULT SYSTEM BLOCK DIAGRAM



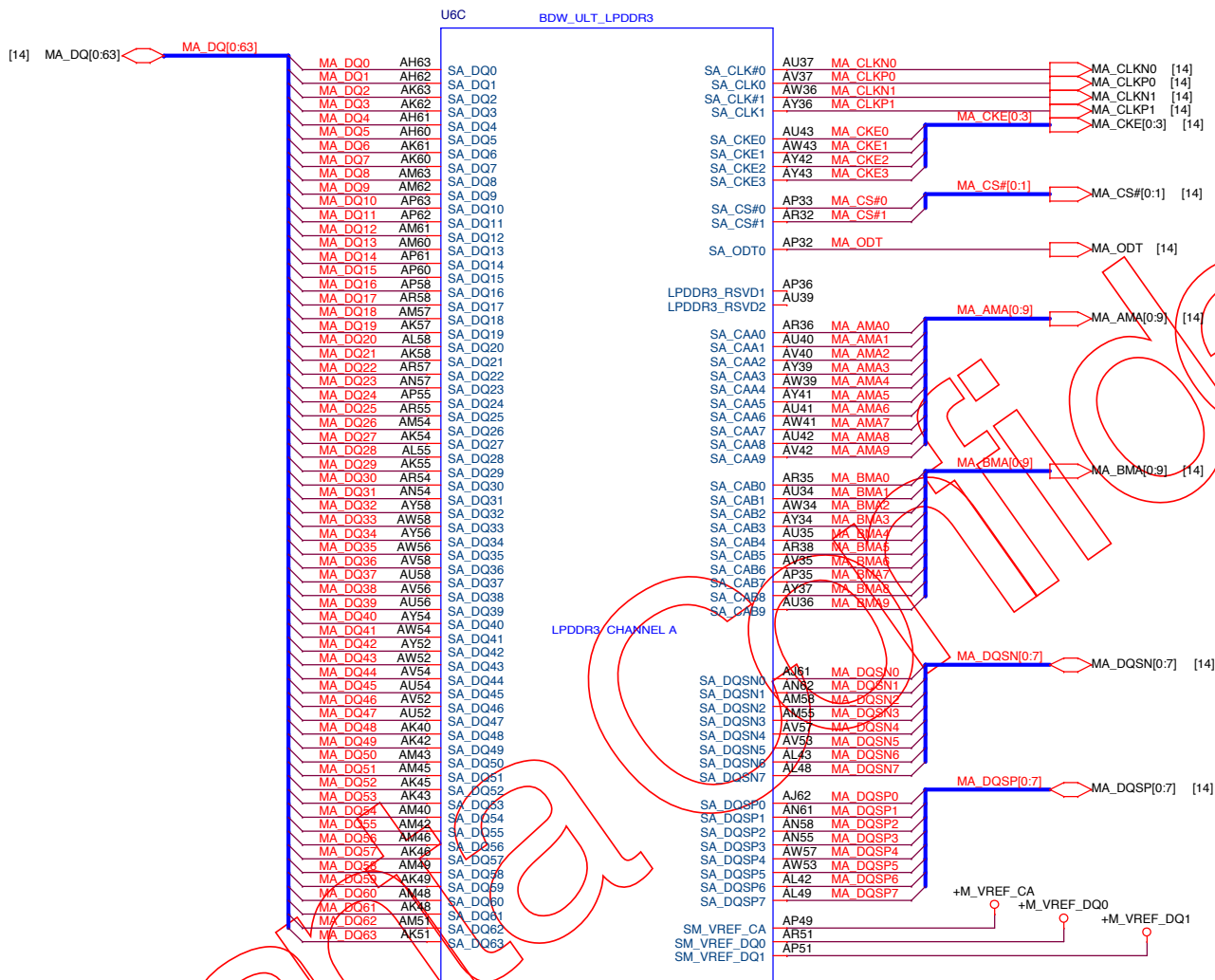




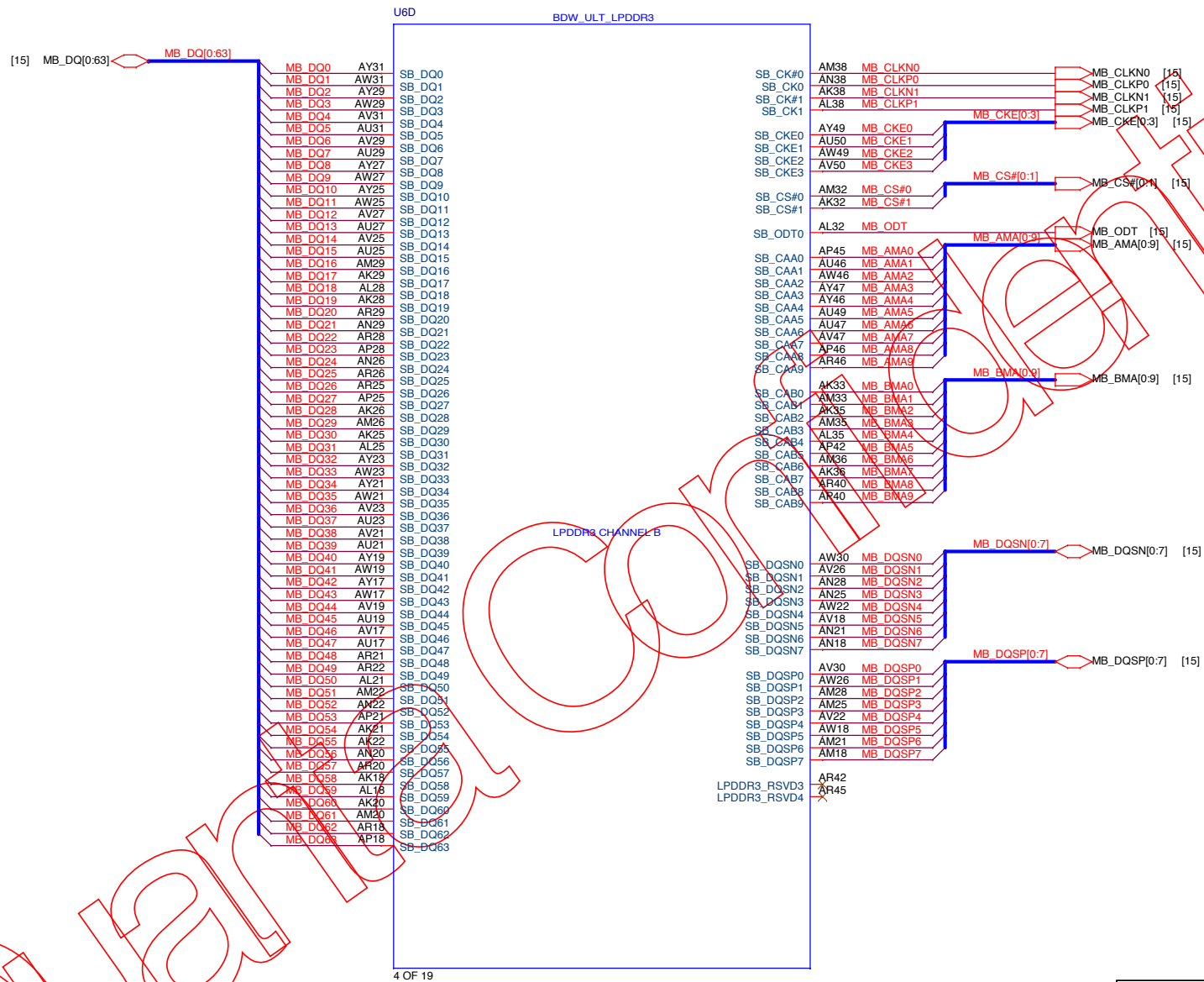
**Quanta Computer Inc.**

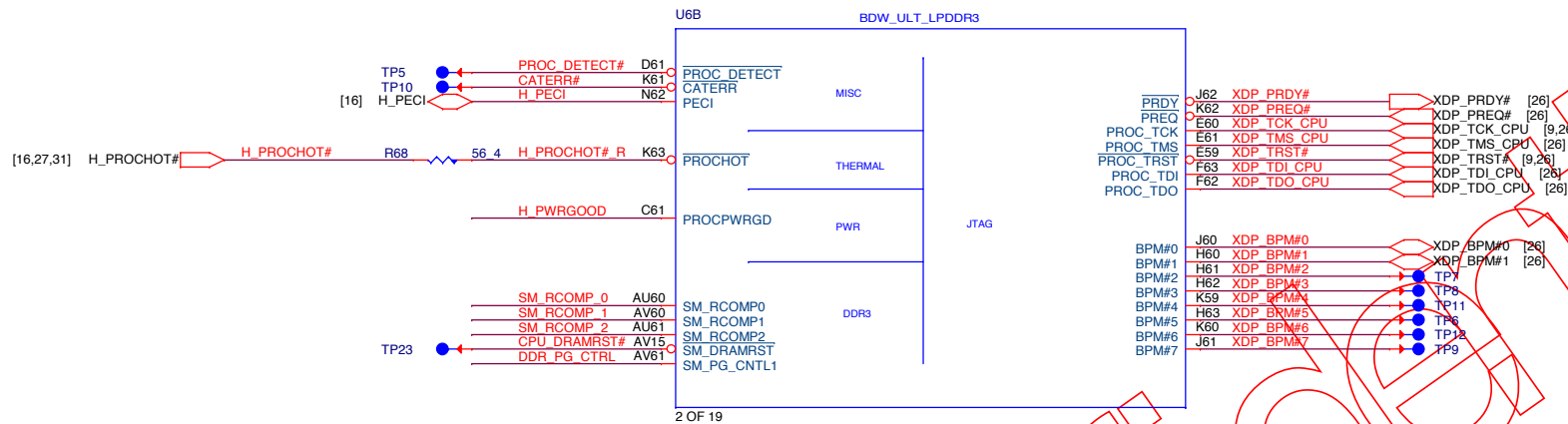
**PROJECT : ZS8**

Size	Document Number	Rev
	<b>BDW Processor (DISPLAY)</b>	1A
Date:	Wednesday, August 13, 2014	Sheet 2 of 35

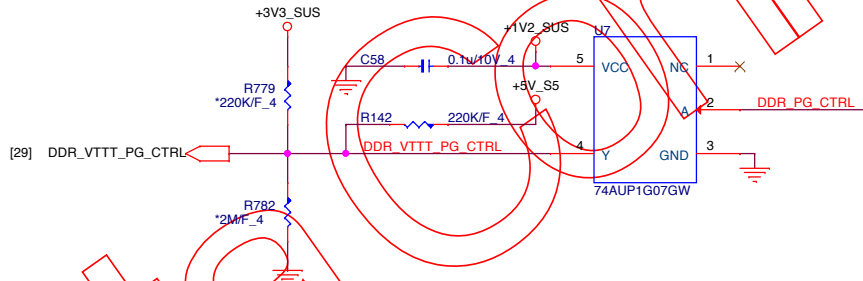
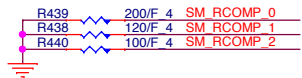


3 OF 19

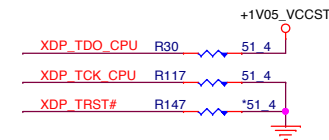




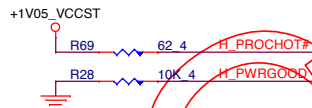
## DRAM COMP



## XDP PU/PD



## PU/PD of CPU

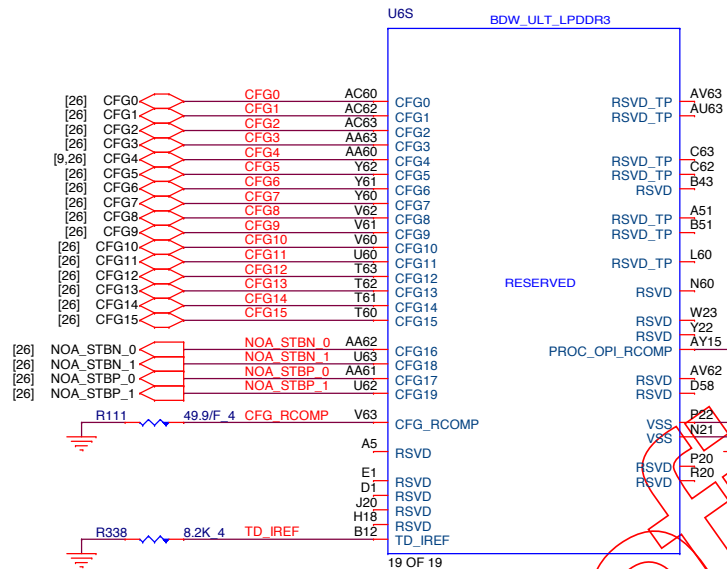


**Quanta Computer Inc.**  
**PROJECT : ZS8**

Size Document Number Rev 1A  
**BDW Processor (SIDE BAND)**  
Date: Wednesday, August 13, 2014 Sheet 5 of 35







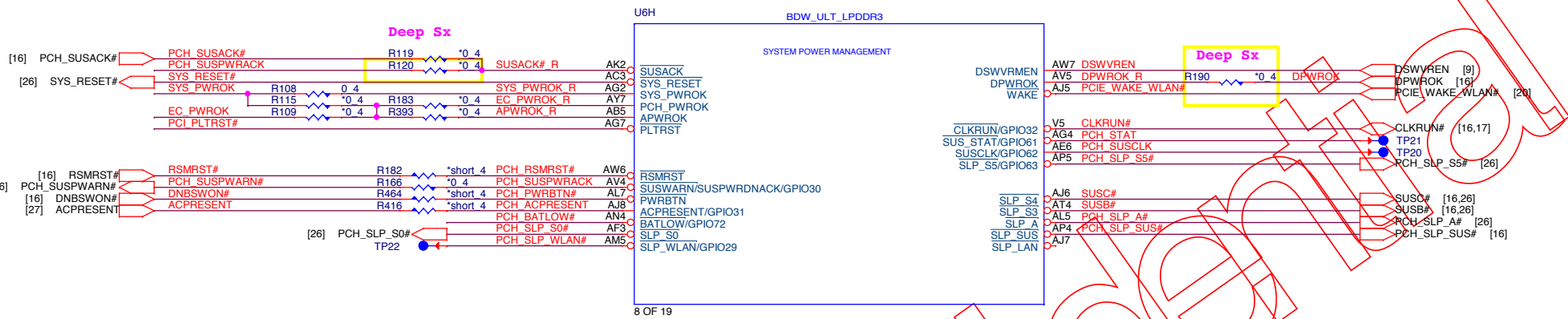
## Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	CFG0 R106 *1K 4
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	CFG1 R105 *1K 4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R104 *1K 4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R100 *1K 4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRs SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R112 *1K 4
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R96 *1K 4

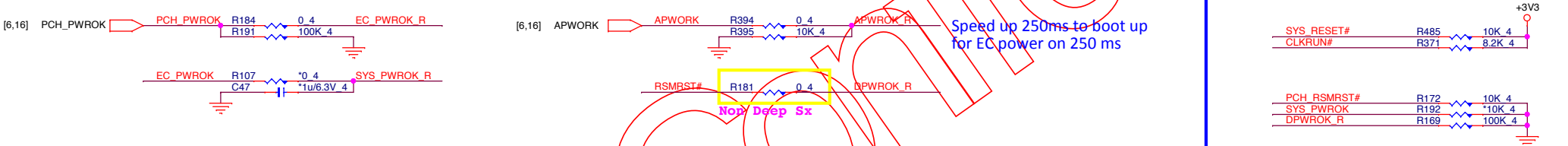


**Quanta Computer Inc.**  
**PROJECT : ZS8**

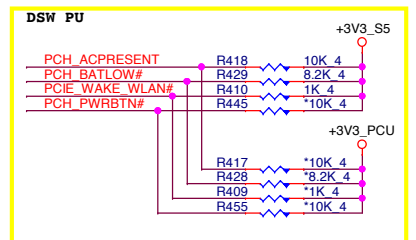
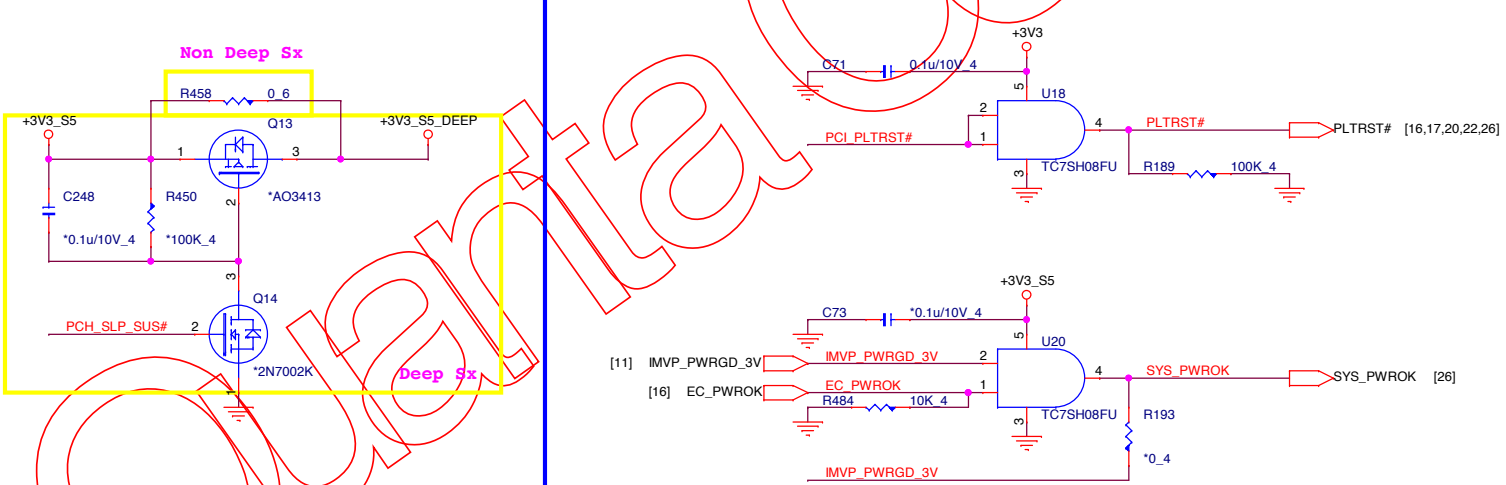
Size	Document Number	Rev
	<b>BDW Processor (CFG)</b>	1A
Date:	Wednesday, August 13, 2014	Sheet 7 of 35



**Power Sequence** **PCH PM PU/PD**



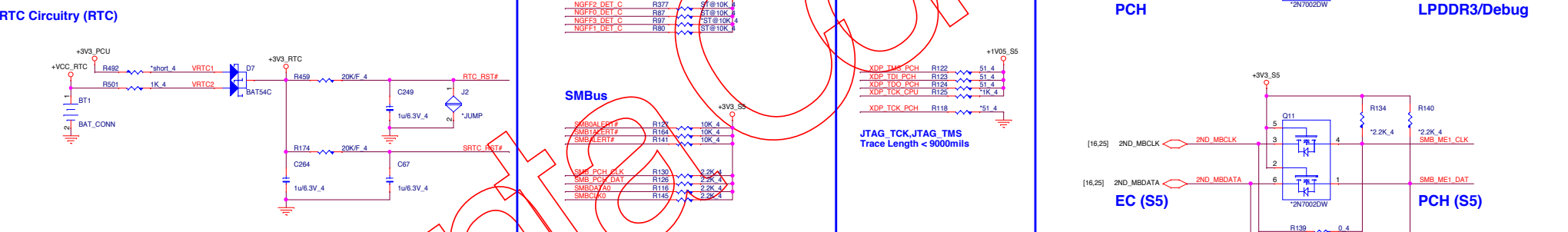
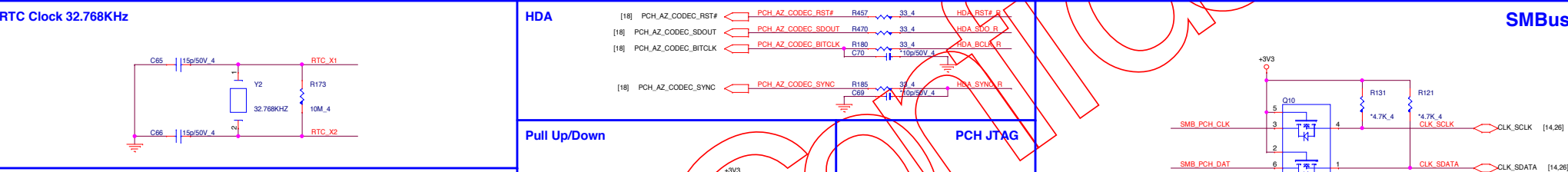
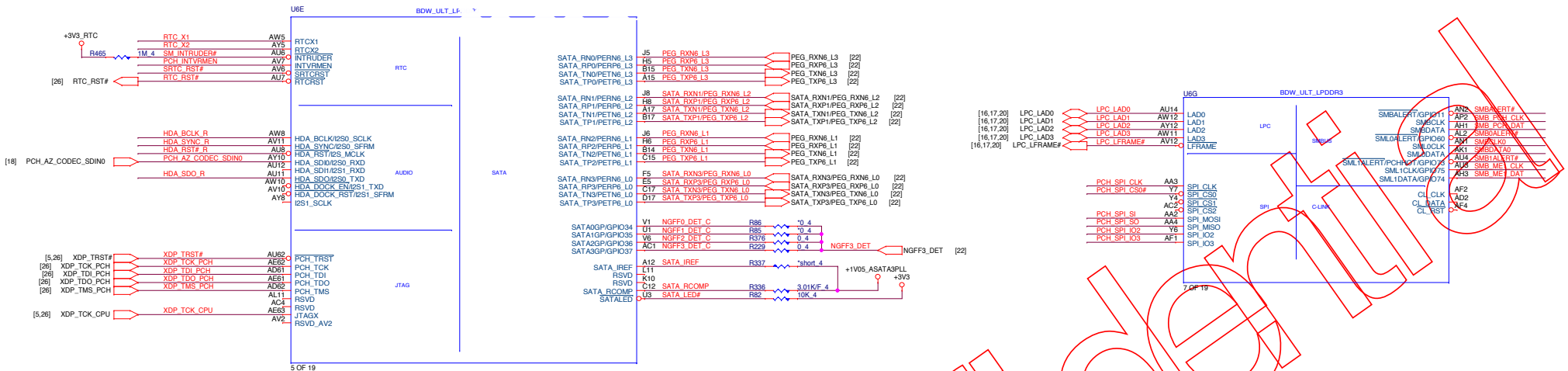
**Deep Sx Circuit** **PLTRST# Buffer**



**Quanta Computer Inc.**  
**PROJECT : ZS8**

Size	Document Number	Rev
	<b>BDW PCH (PM)</b>	1A
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ULT Strapping Table			
Pin Name	Strap description	Sampled	Configuration
GPIO81(SPKR)	No reboot on TCO Timer expiration	PWROK	0 = Default enable (IPD 20K) 1 = Disable No-Reboot mode
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Default can program ME (IPD 20K) 1 = can't program ME
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	1 = Should be always pull-up
GPIO66	Top-Block Swap override		0 = Default disable (IPD 20K) 1 = Enable TBS function
GPIO86	Boot BIOS Strap Bit		0 = Default SPI (IPD 20K) 1 = LPC
GPIO15	TLS(Transport layer security)		0 = Default enable w/o confidentiality (IPD 20K) 1 = Default enable with confidentiality
CFG4	DP presence strap		0 = Enable an external display port is connected to the eDP 1 = disable
DSWVREN	Deep Sx well on the VR enable		1 = Should be always pull-up

Pull Up/Down			
+3V3	R88	*1K_4	SPKR [11,18]
+3V3_RTC	R179	330K_4	PCH_INTVRMEN
+3V3	R20	*1K_4	GPIO66 [11]
+3V3	R345	*1K_4	GPIO86 [11]
+3V3_S5	R403	8.2K_4	GPIO15 [11]
+3V3	R103	*1K_4	CFG4 [7,26]
+3V3_RTC	R178	33K_4	DSWVREN [8]

PCH Quad SPI ROM(8M) (CPU)			
[16] SPI_CS0#_UR_ME	R482	10K_4	PCH_SPI_CS0#
[16] PCH_SPI_SO_EC	R489	*short_4	PCH_SPI_SO_R
[16] PCH_SPI_SI_EC	R478	*1K_4	PCH_SPI_SI_R
[16] PCH_SPI_CLK_EC	R448	*short_4	PCH_SPI_CLK_R

Vendor	W25Q64FVSS10	AKS3EPF0N07
Winbond	BN25Q64-104H1P	AKS3EPN0Q01
GD	GD25Q64B51GX	AKS3EPN0Q01

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Sheet	9 of 35	Rev 1A

NGFF  
SSD0

Wlan

MB USB3.0

MB USB3.0

DB USB2.0

BlueTooth

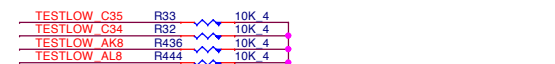
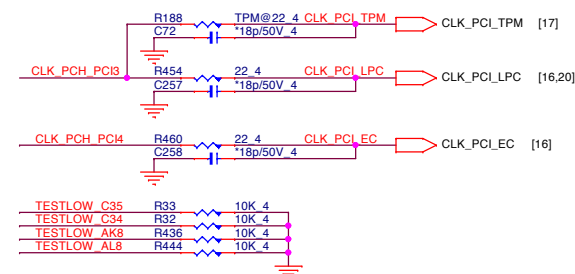
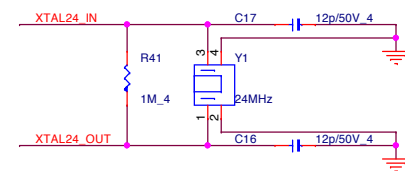
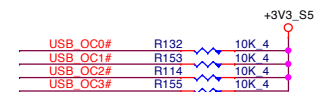
Touch Screen

CCD

Card Reader

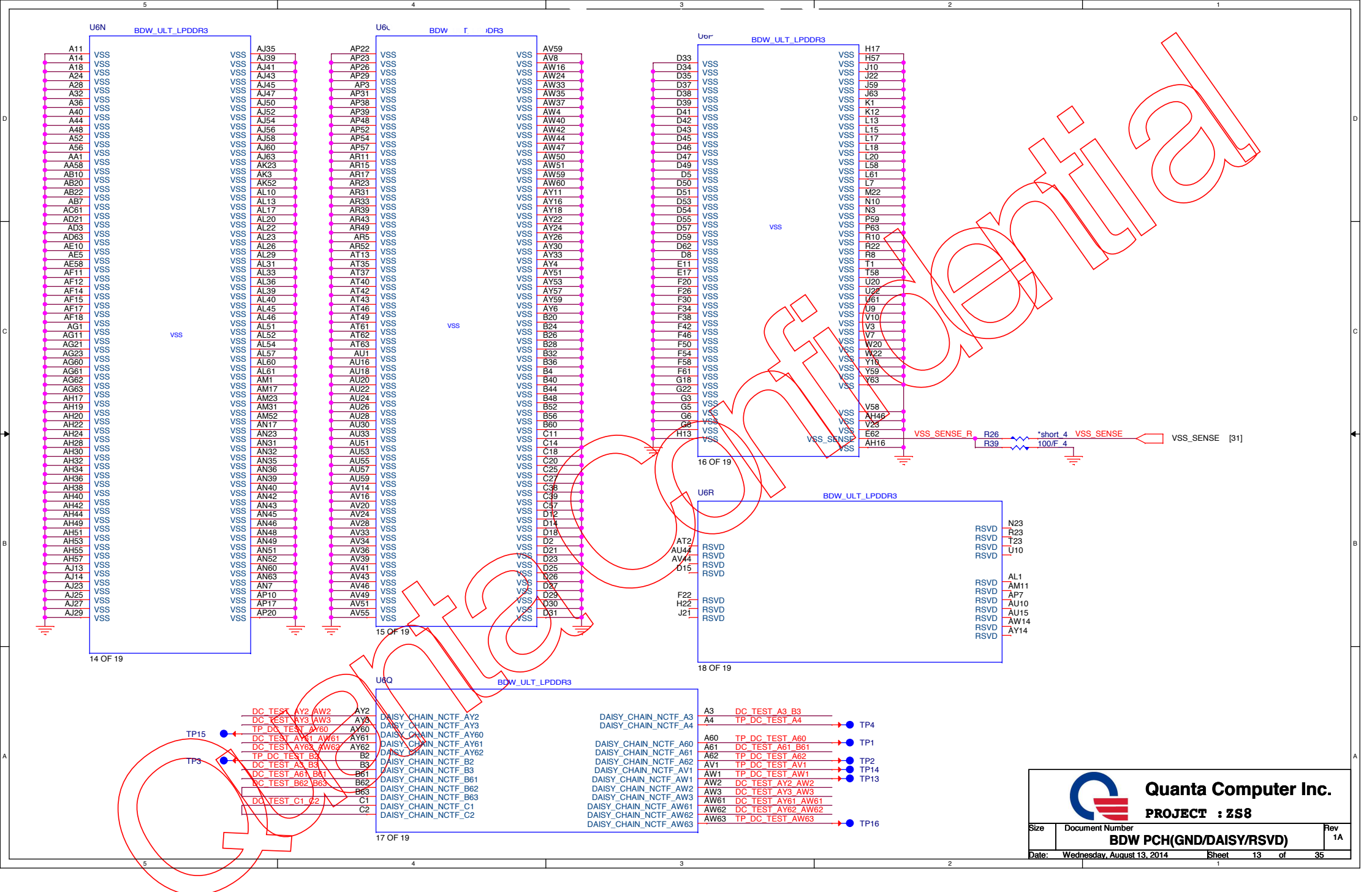
MB USB3.0

MB USB3.0



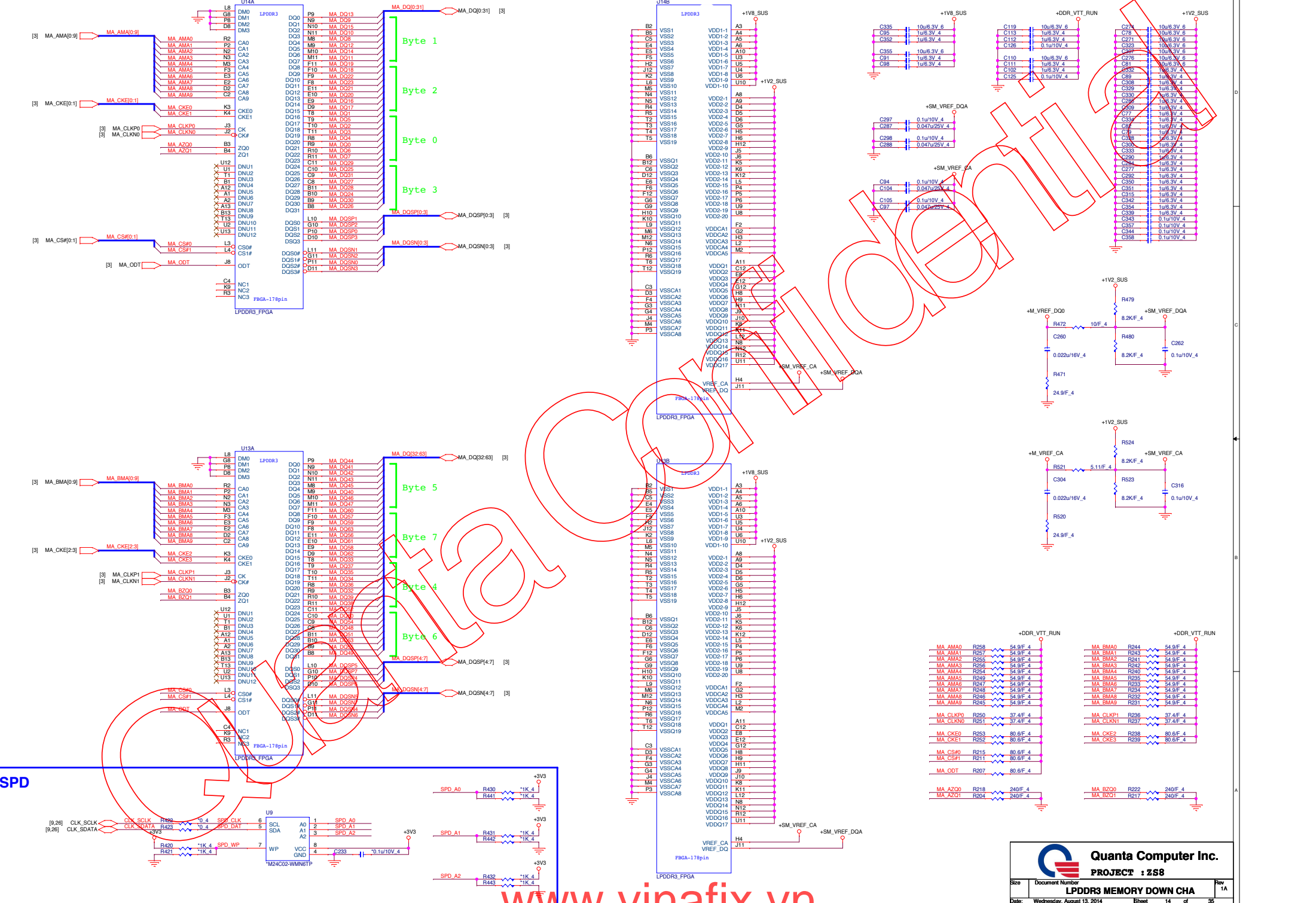






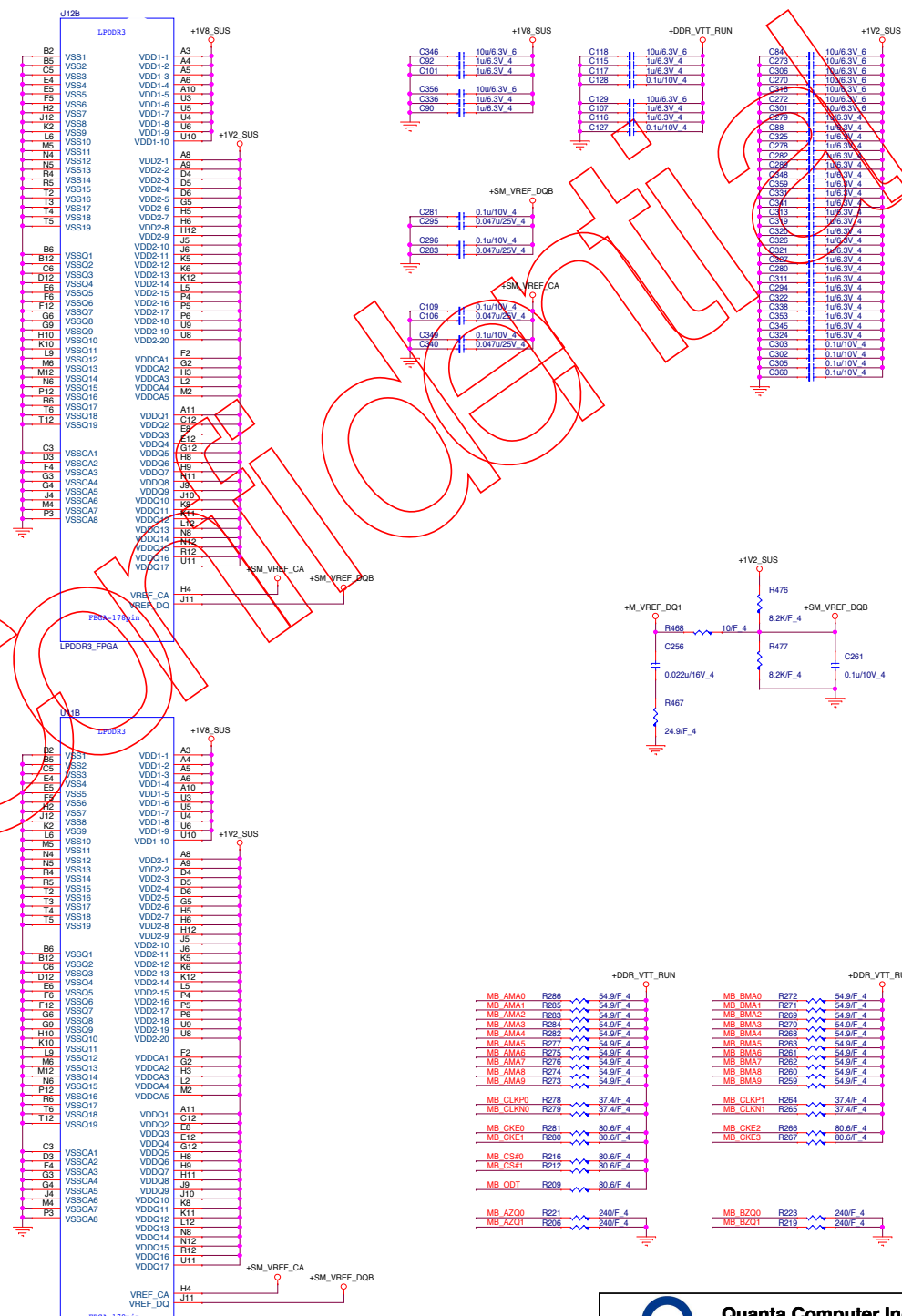
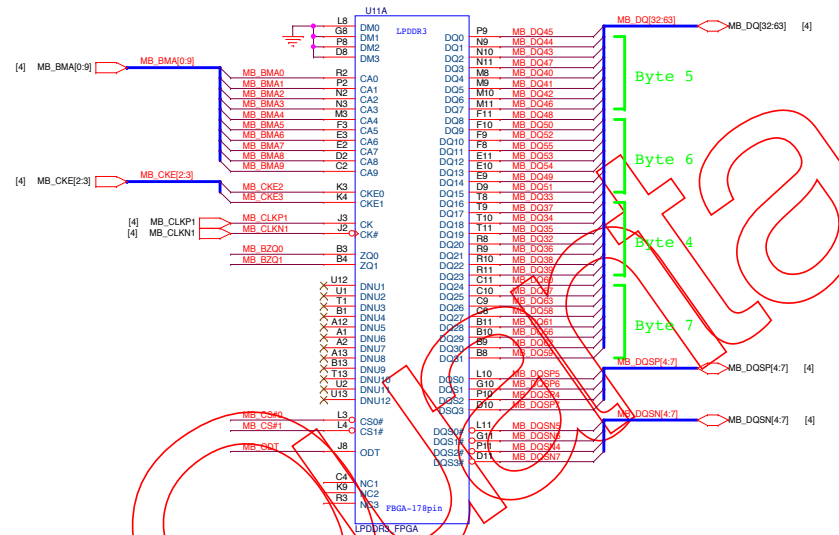
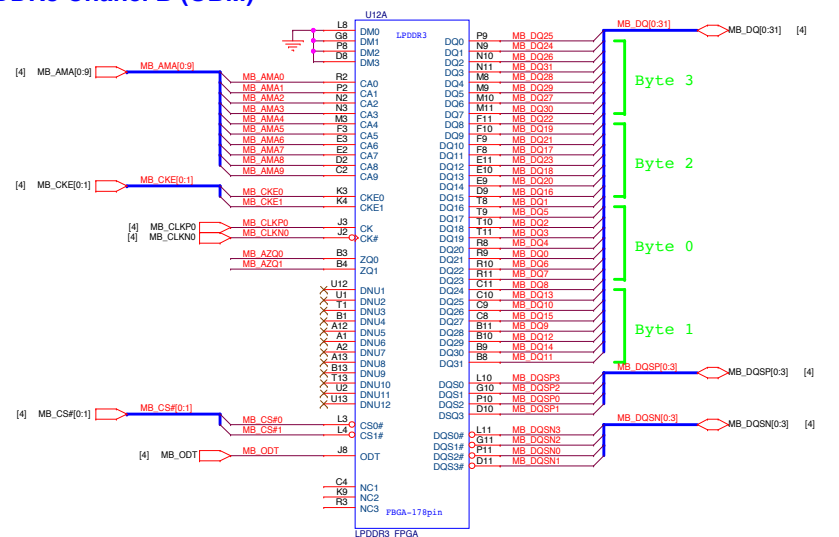


LPDDR3 Chane A (OBM)

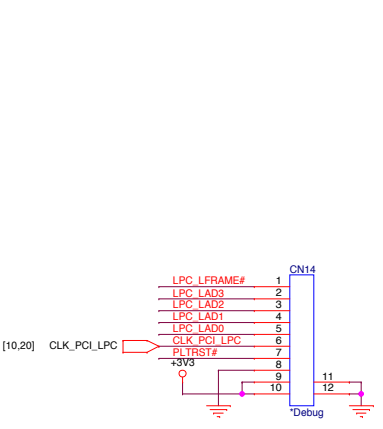
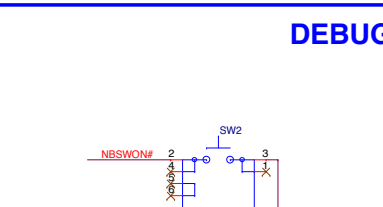
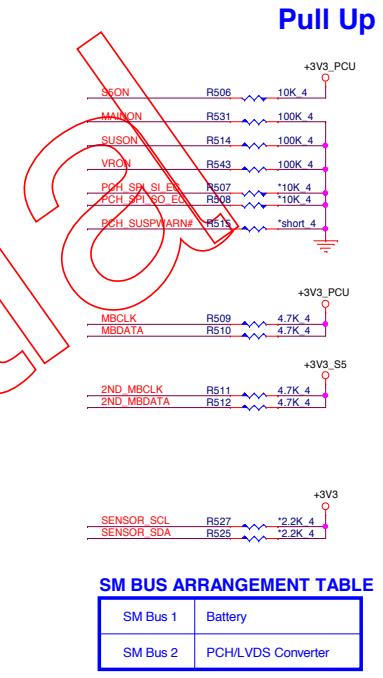
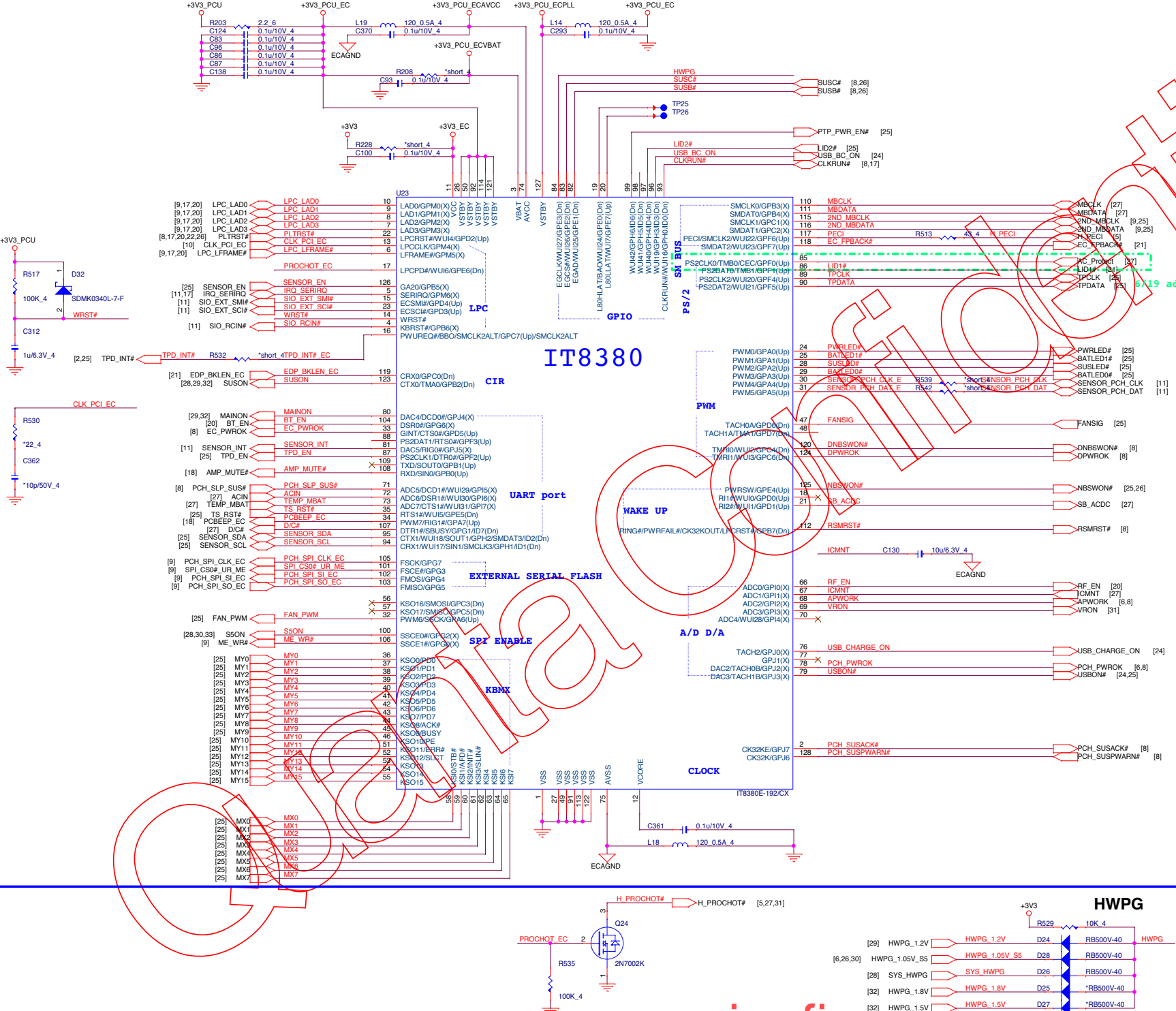




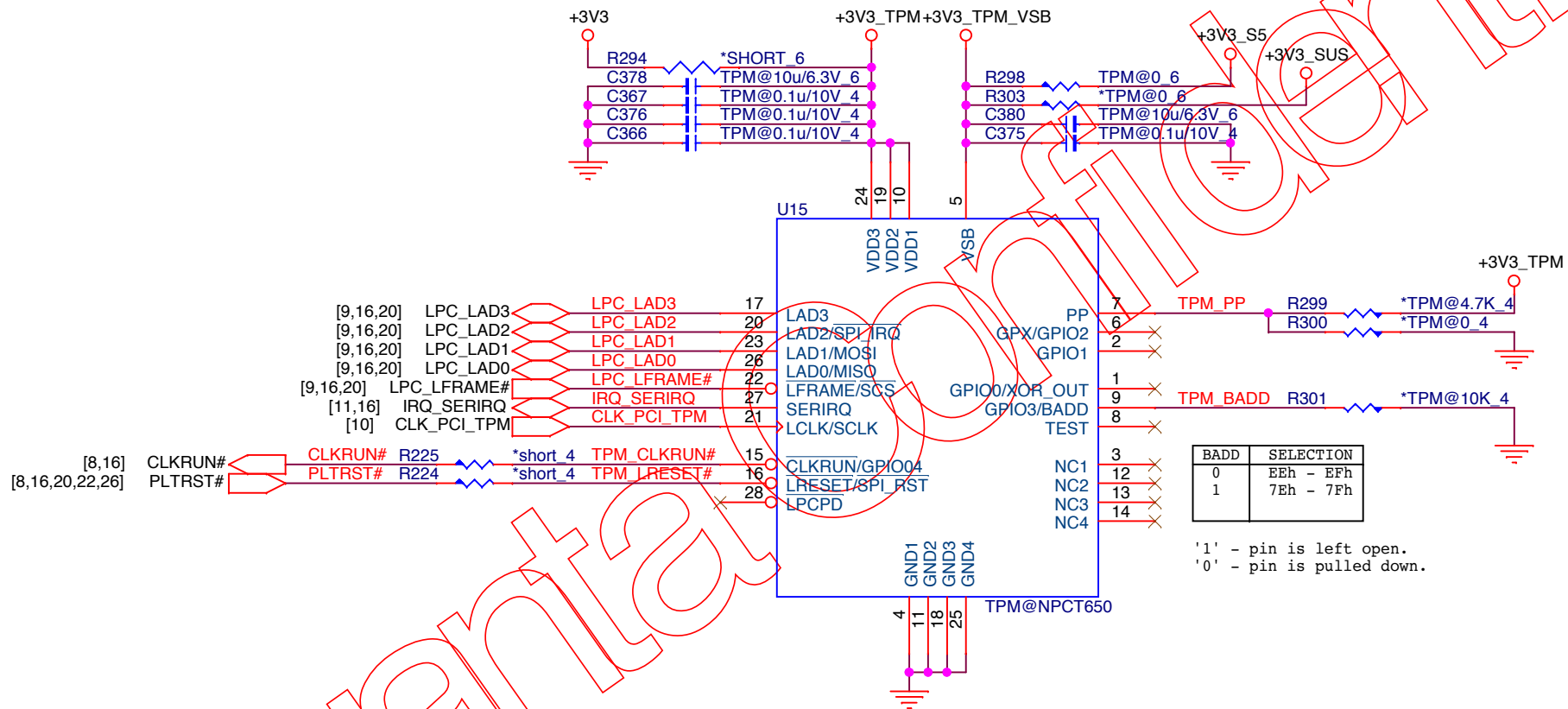
### LPDDR3 Chanel B (OBM)



# EC IT8380 (KBC)



# TPM NPCT650 (TPM)



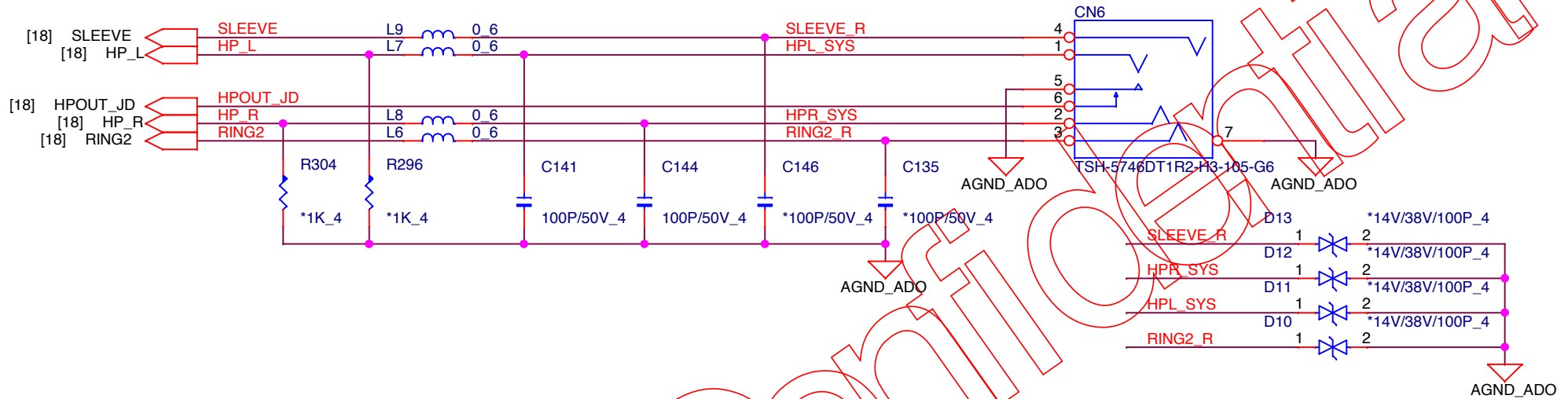
**Quanta Computer Inc.**

**PROJECT : ZS8**

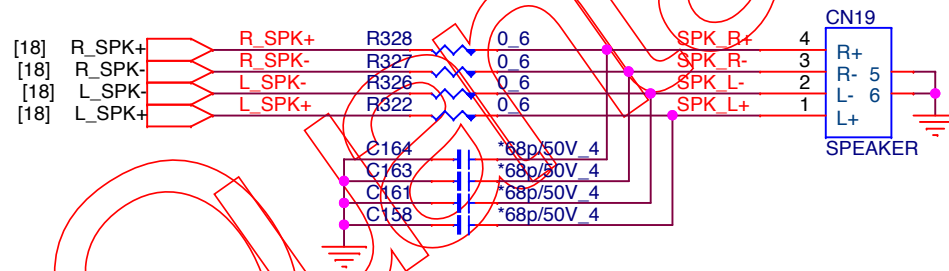
Size	Document Number	Rev
	<b>NPCT650</b>	<b>1A</b>
Date:	Wednesday, August 13, 2014	Sheet 17 of 35



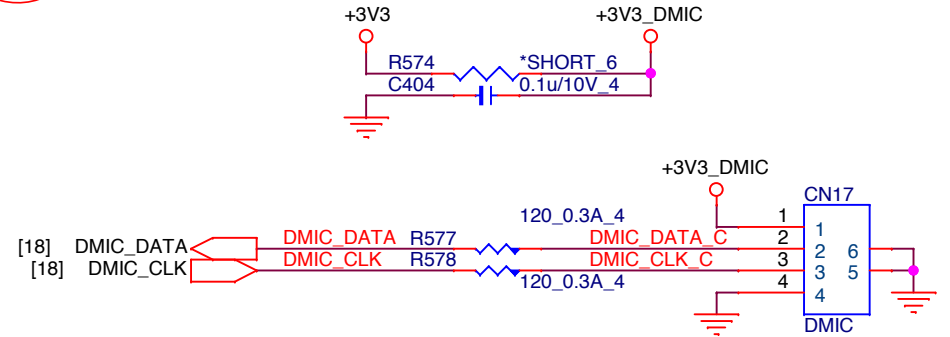
## Universal Audio Jack (ADO)



## Speaker (ADO)



## DMIC (ADO)

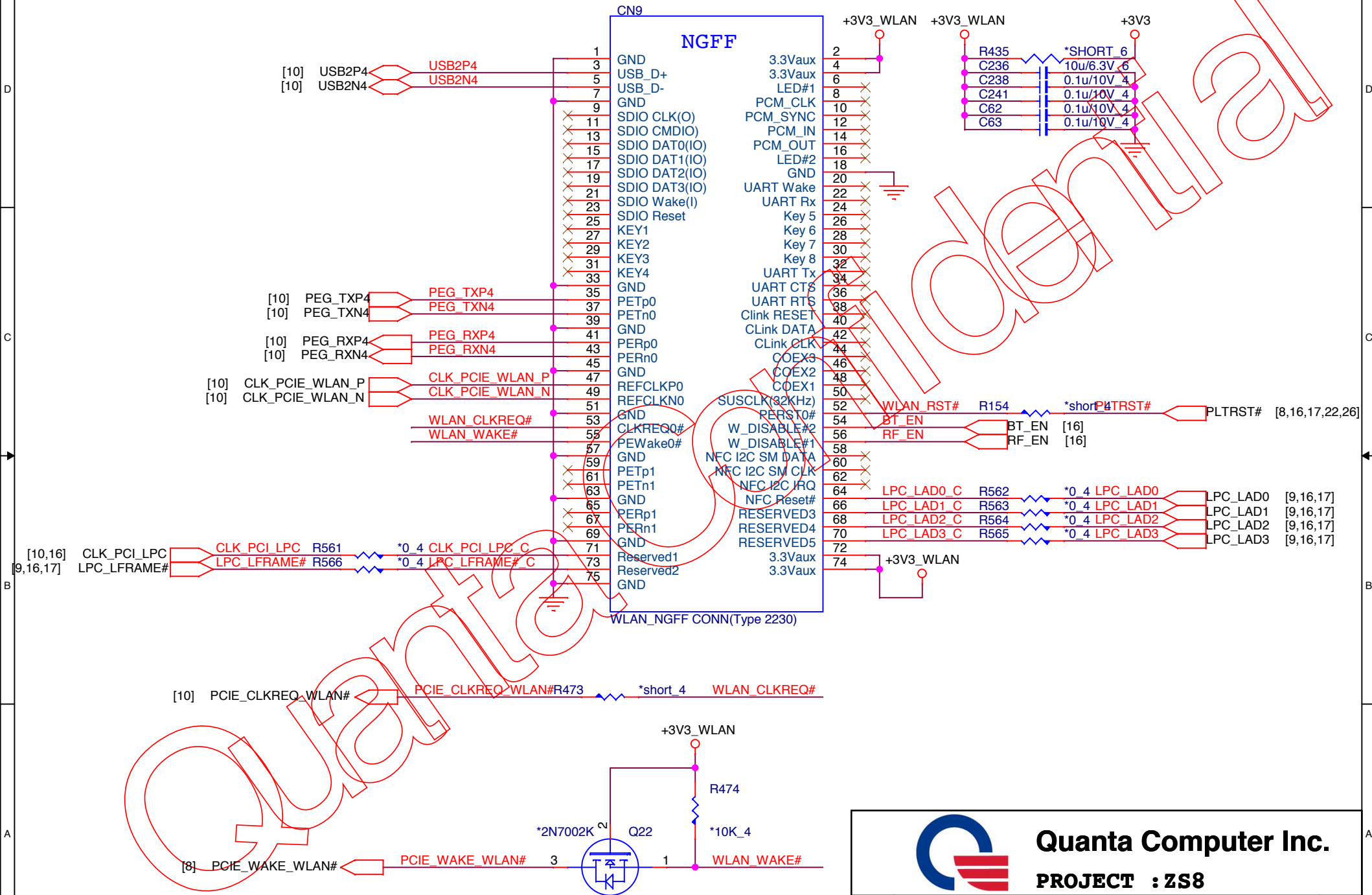


**Quanta Computer Inc.**

**PROJECT : ZS8**

Size	Document Number	Rev
	<b>Audio Jack/Speaker/DMIC</b>	<b>1A</b>
Date:	Wednesday, August 13, 2014	Sheet 19 of 35

## NGFF WiFi & BT (NGF)



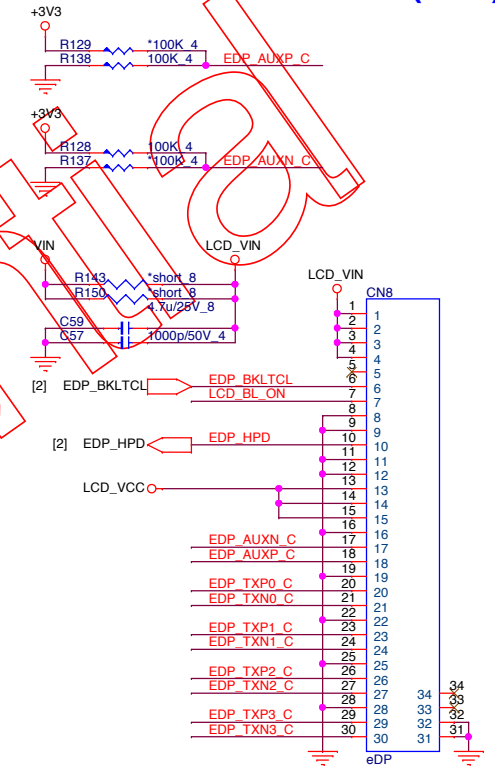
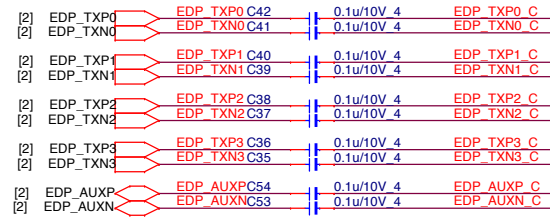
**Quanta Computer Inc.**

**PROJECT : ZS8**

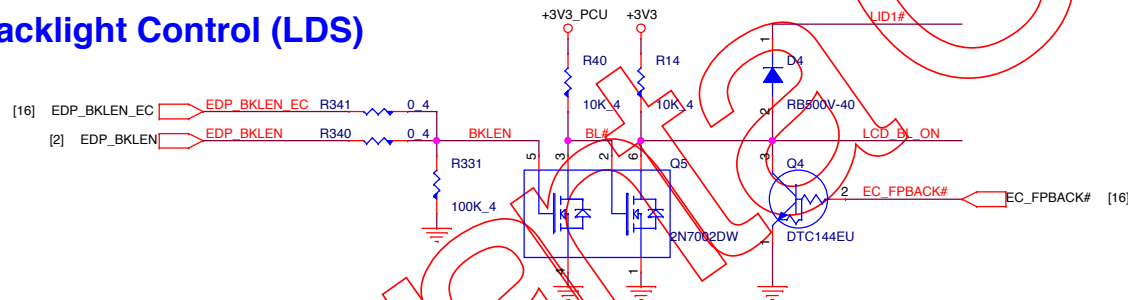
Size	Document Number	Rev
	<b>NGFF WiFi &amp; BT</b>	<b>1A</b>
Date:	Wednesday, August 13, 2014	Sheet 20 of 35



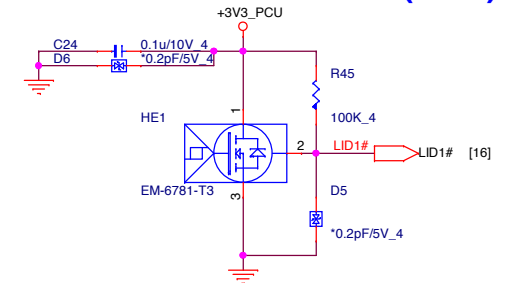
## eDP Connector (LDS)



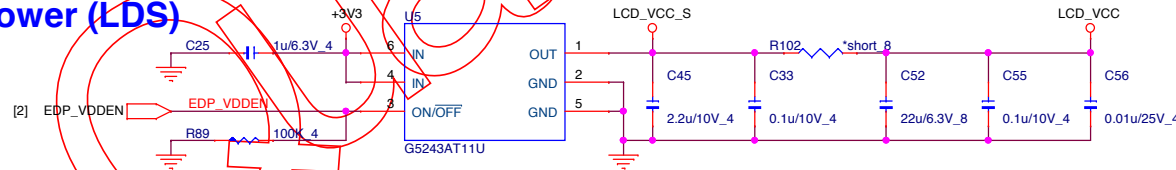
## Backlight Control (LDS)



## Hall Sensor (HSR)



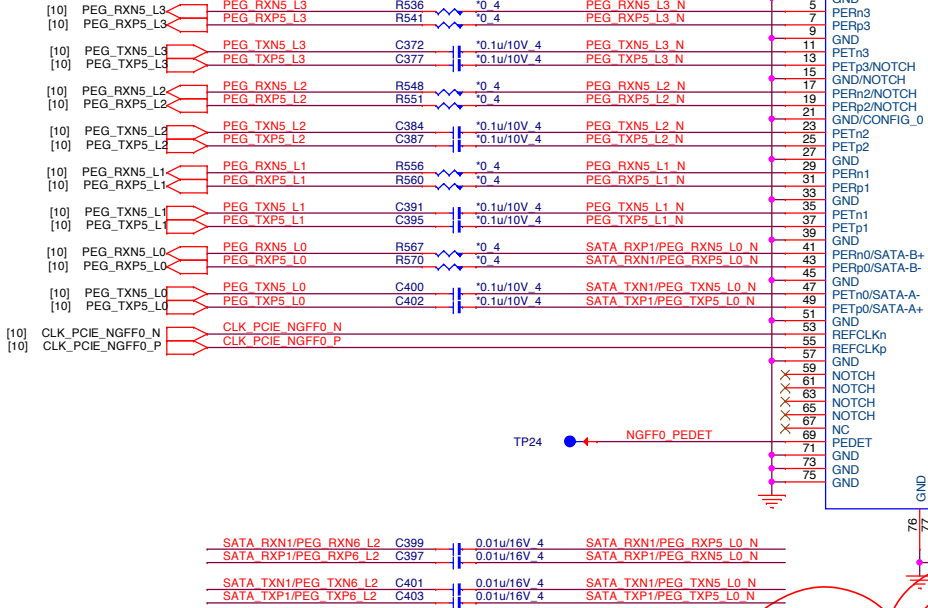
## eDP Power (LDS)



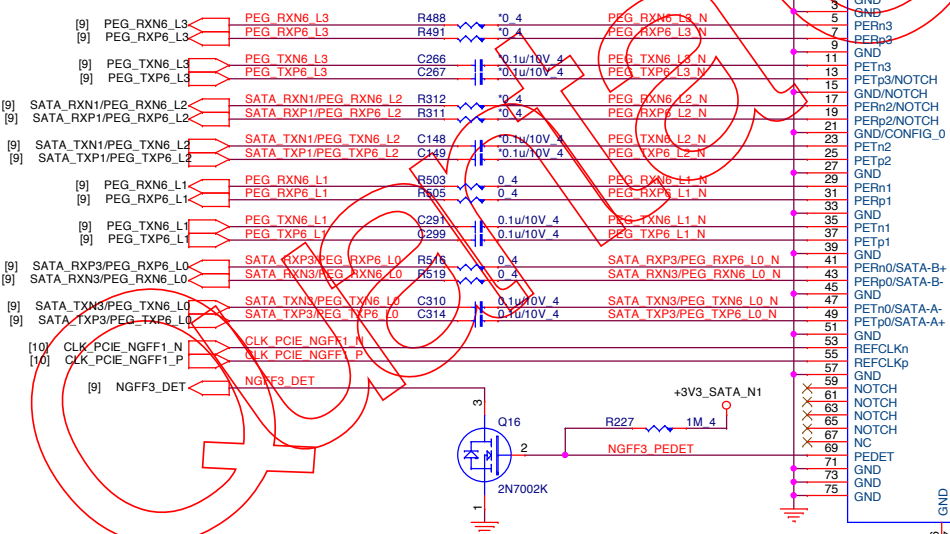
**Quanta Computer Inc.**  
**PROJECT : ZS8**

Size	Document Number	Rev
	eDP/redriver/Hall	1A
Date:	Wednesday, August 13, 2014	Sheet 21 of 35

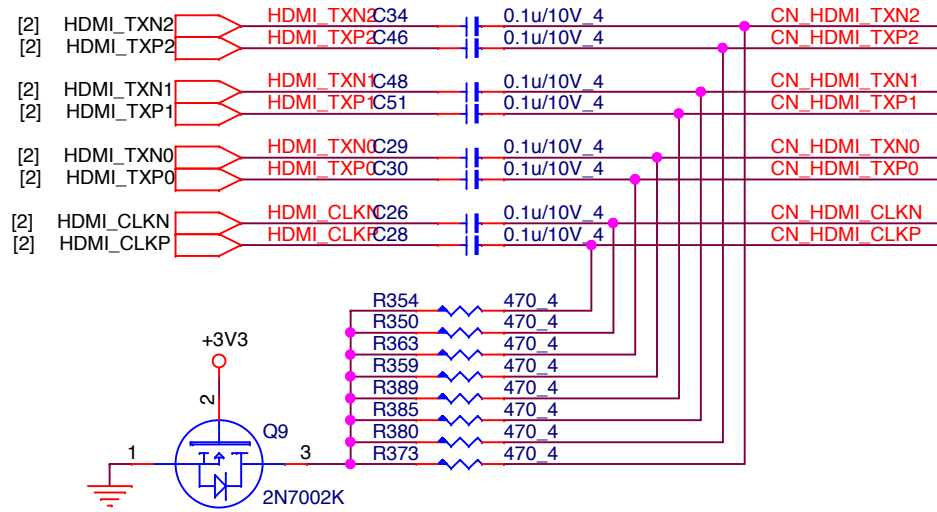
## NGFF SATA1/PEG5 (NGF)



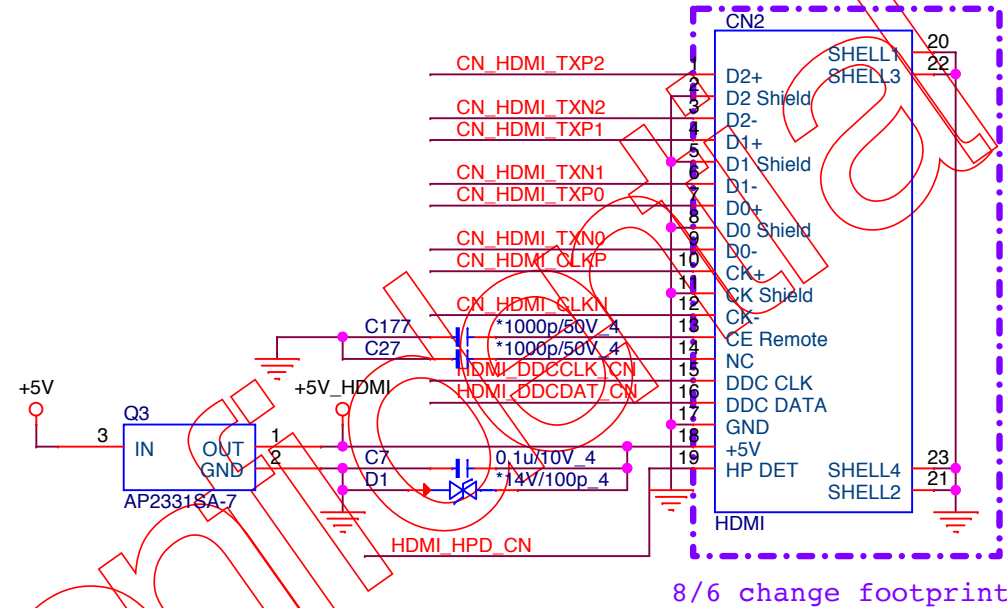
## NGFF SATA3/PEG6 (NGF)



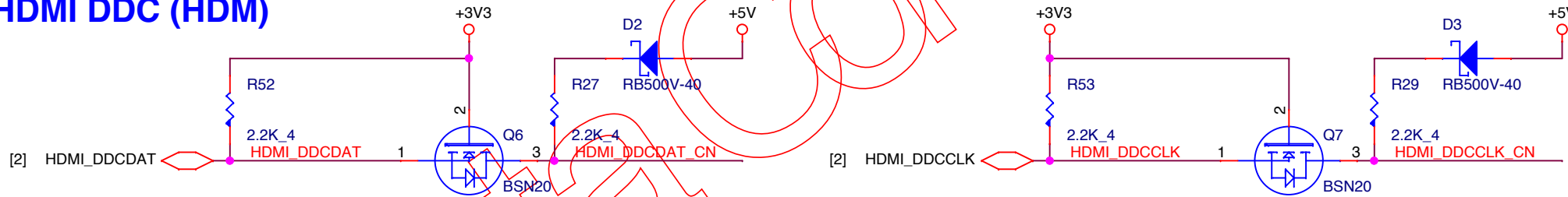
## HDMI Cost Reduced level shift (HDM)



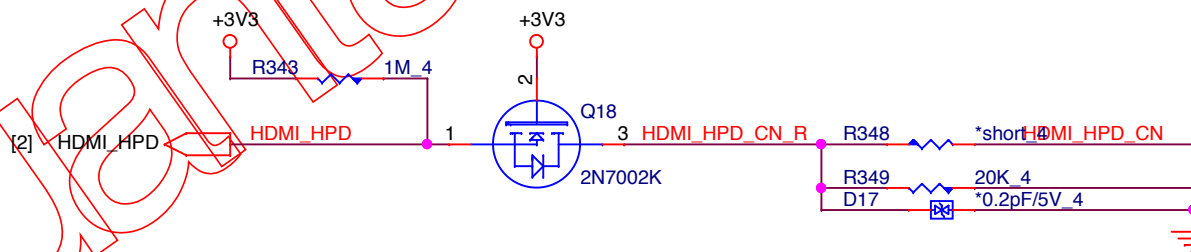
## HDMI connector (HDM)



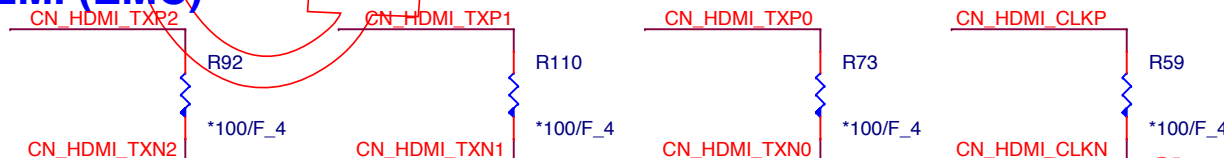
## HDMI DDC (HDM)



## HDMI-detect (HDM)



## EMI (EMC)

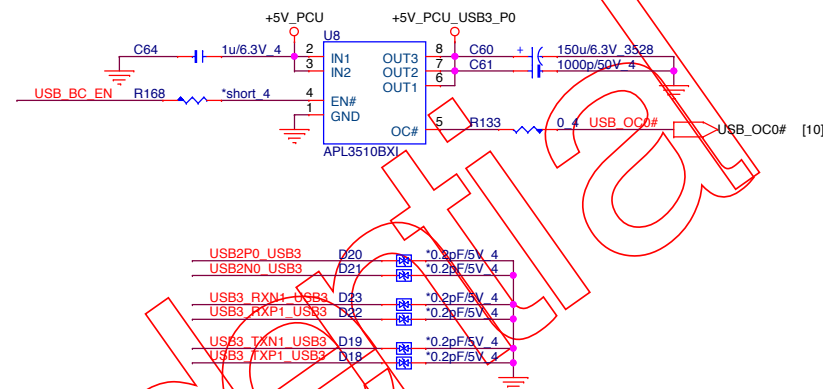


Quanta Computer Inc.

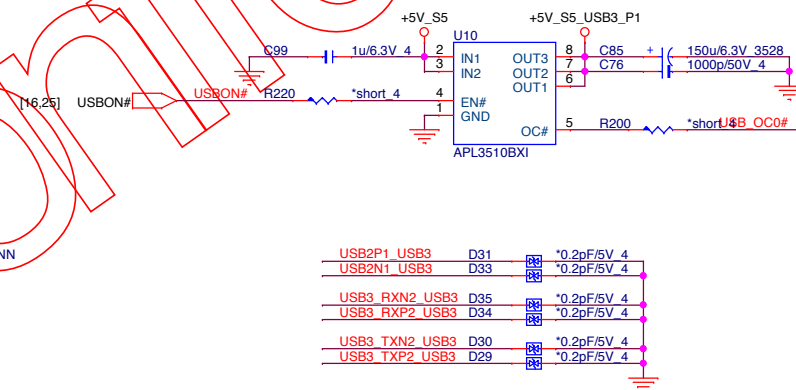
PROJECT : ZS8

Size	Document Number	Rev
	HDMI	1A
Date:	Wednesday, August 13, 2014	Sheet 23 of 35

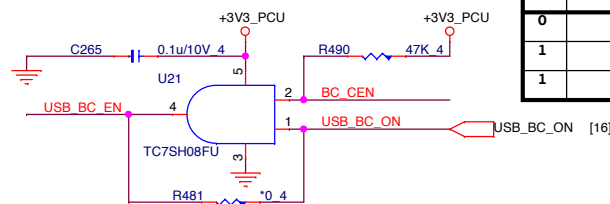
### USB 3.0 Port0 (UB3)



### USB 3.0 Port1 (UB3)



## USB Charger for USB3.0 Port0 (UBC)



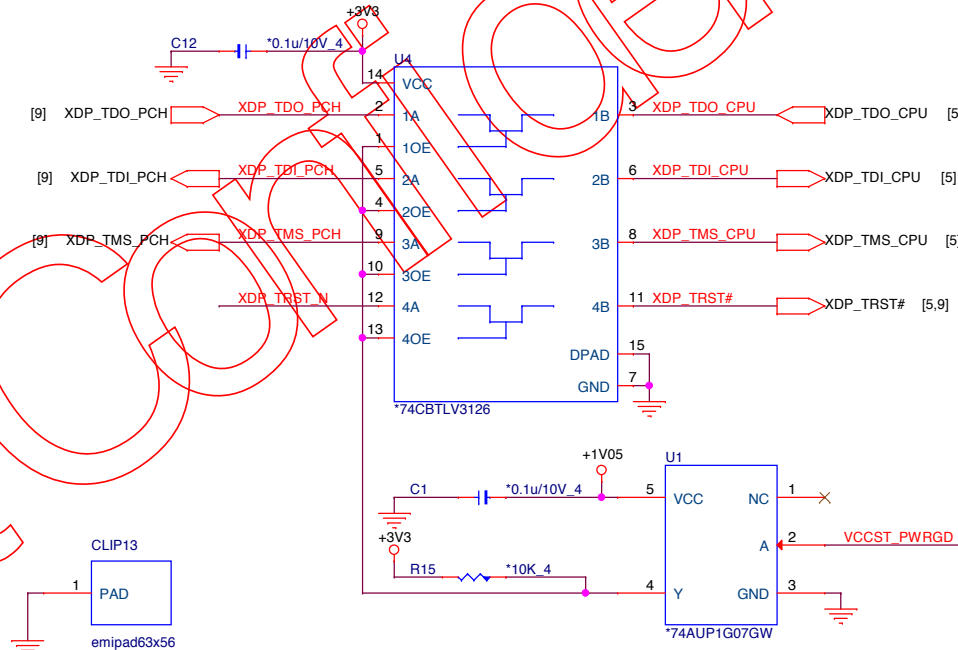
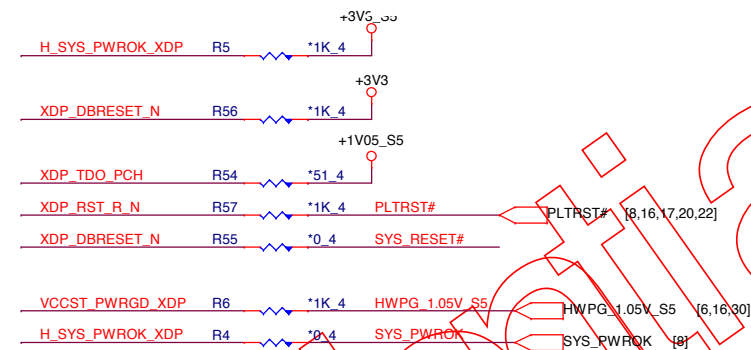
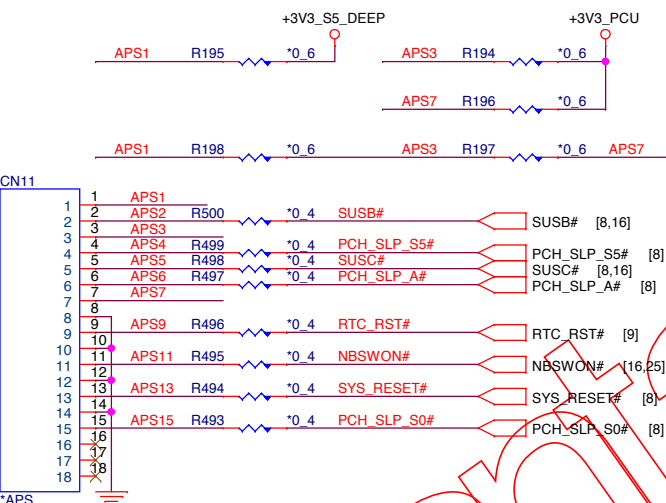
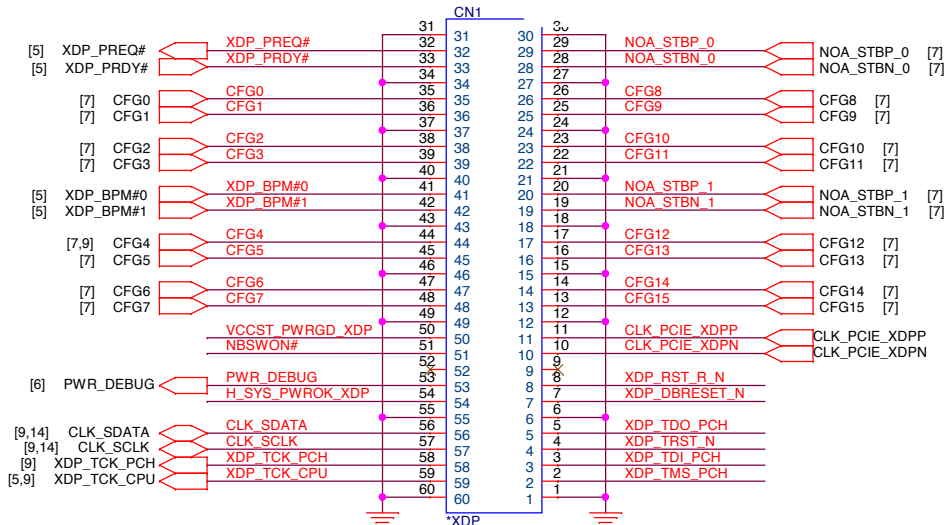
CB	SELCDP	Funcion
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external de



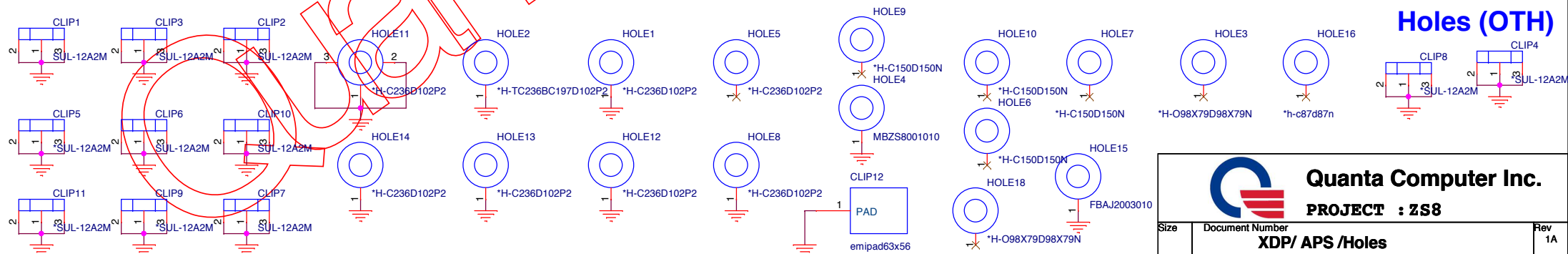
Size	Document Number <b>USB3.0/FAN</b>	Rev 1A
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# XDP/ APS (CPU)



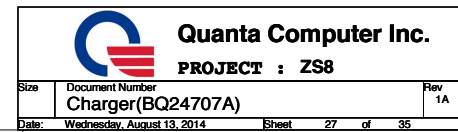
## Holes (OTH)

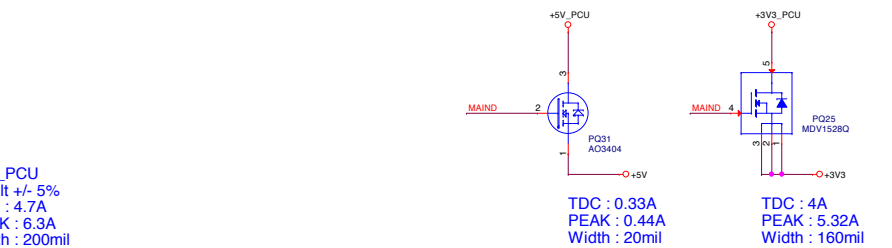
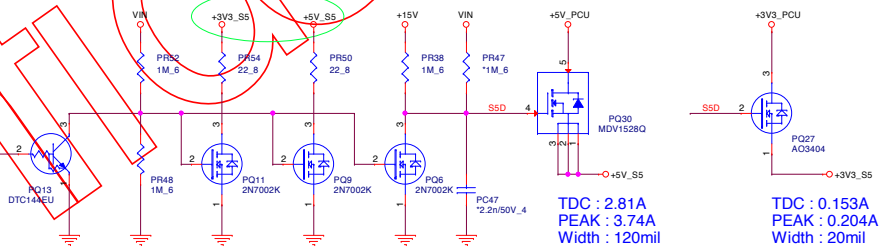
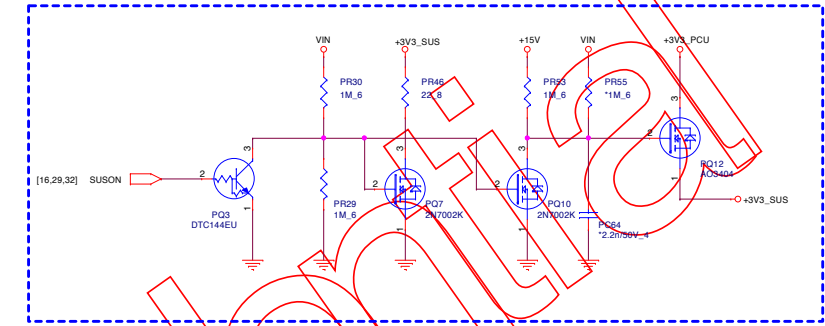
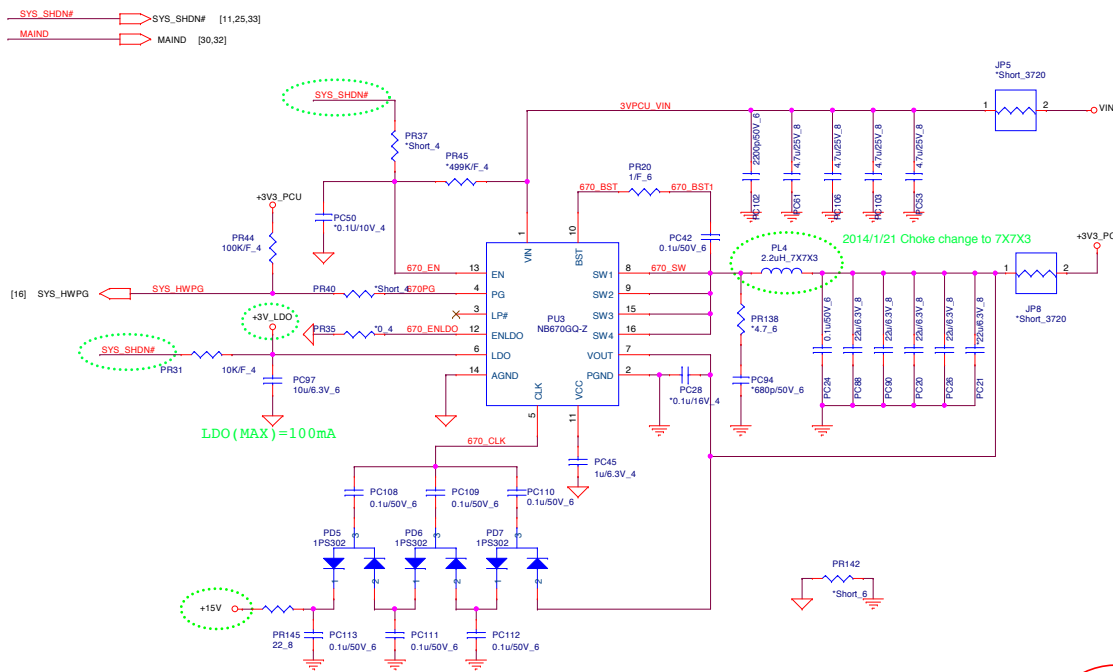


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PROJECT : ZS8

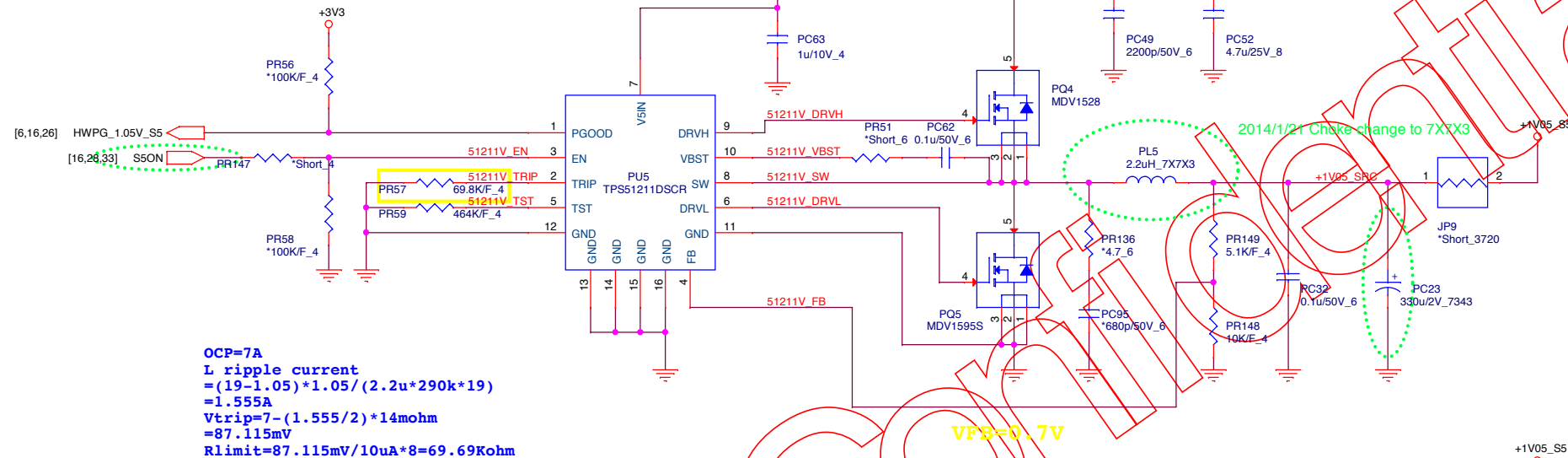
Size	Document Number	Rev
	XDP/ APS /Holes	1A
Date:	Wednesday, August 13, 2014	Sheet 26 of 35



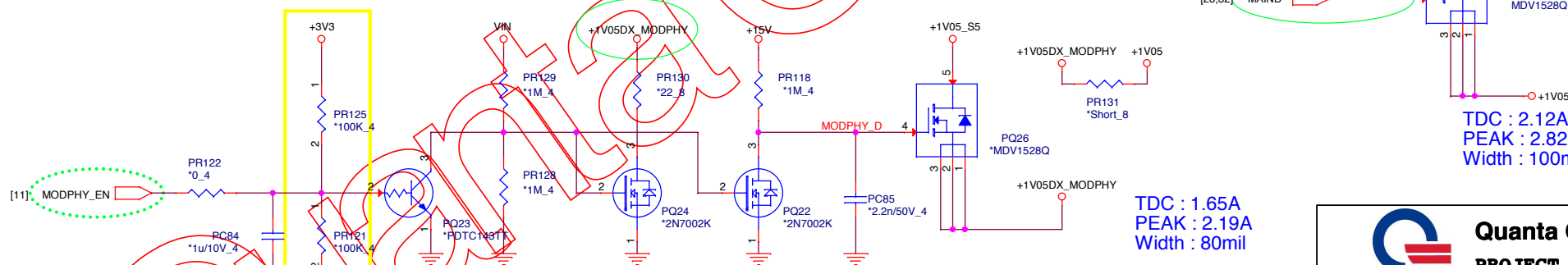







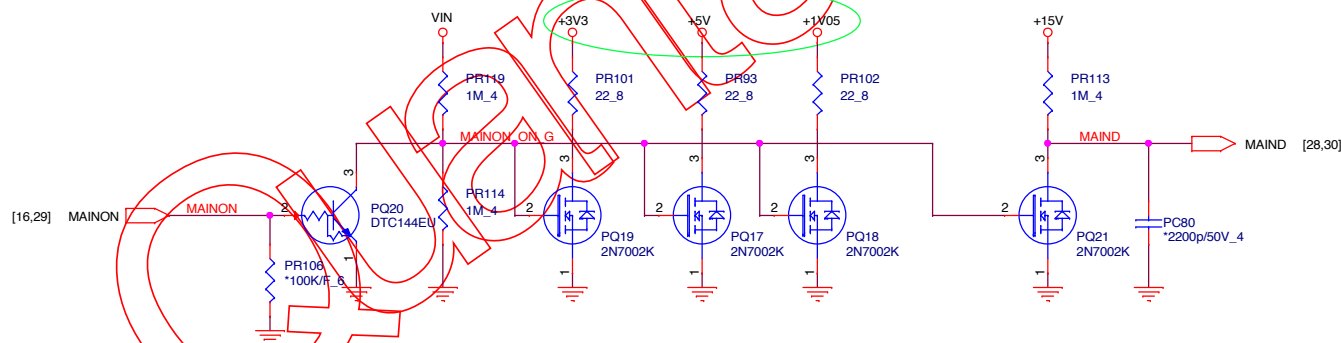
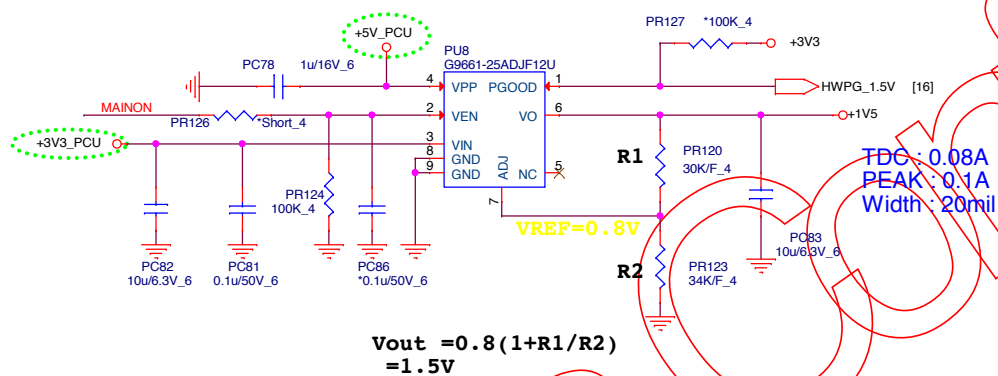
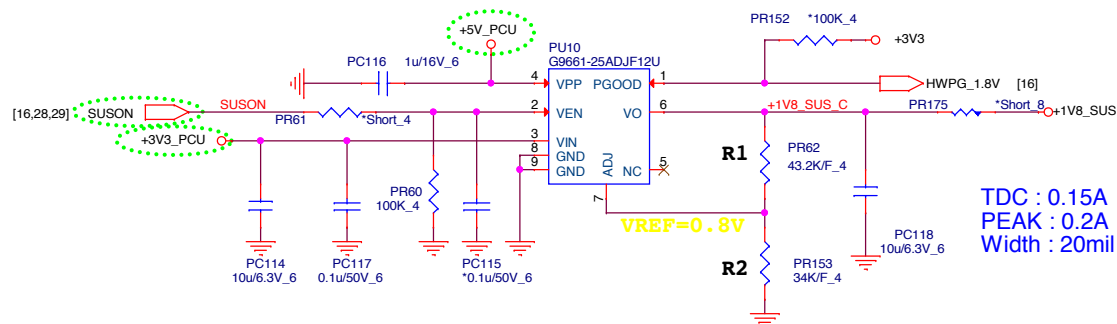


## 12/27 Sequence Modify



 <b>Quanta Computer Inc.</b> <b>PROJECT : ZS8</b>			
Size	Document Number	Rev	
	<b>+1V05_S5 (TPS51211)</b>	1A	
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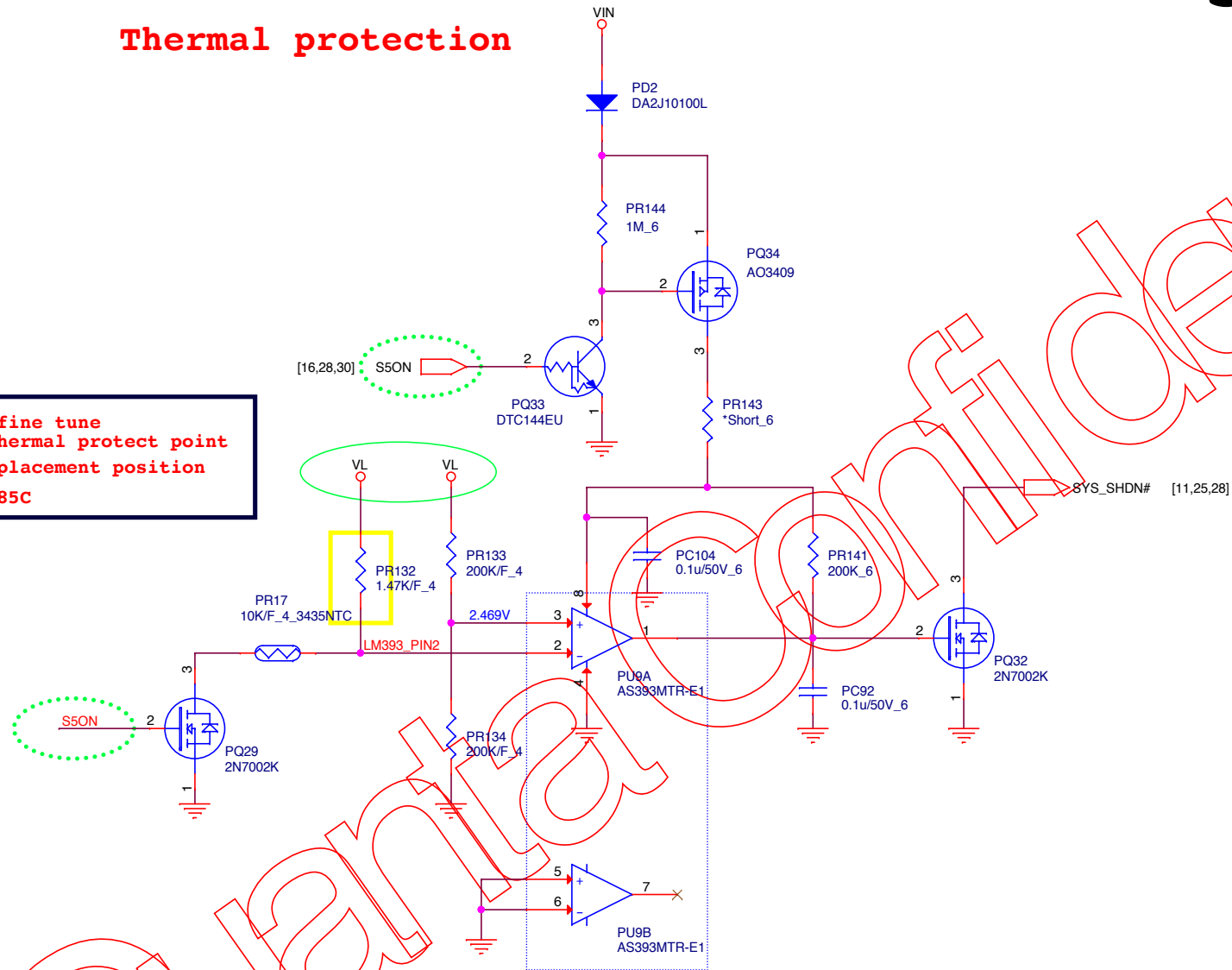
PROJECT : ZS8

Size	Document Number	Rev
	+1.5V/+1.8V	1A
Date	Wednesday, August 13, 2014	Sheet 32 of 35



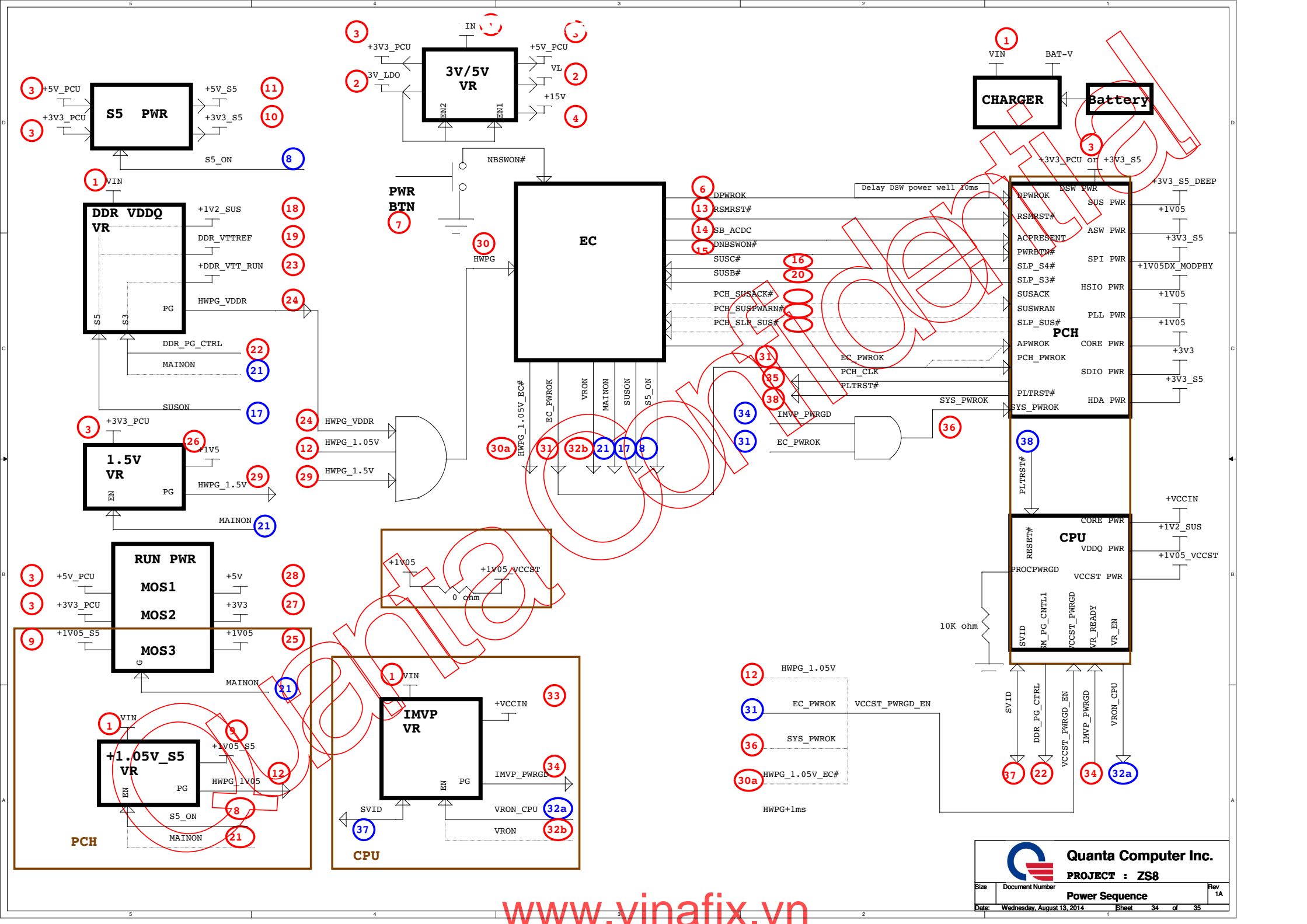
## Thermal protection

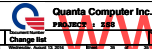
Need fine tune  
for thermal protect point  
Note placement position  
TEMP=85C



**For EC control thermal protection (output 3.3V)**





Model	Version	CHANGE LIST
ZS8	B	
	302	page 11: add R777J878J79 pull high PWR well +V3_3S for electric leakage page 22: change Q16 pull high PWR well to +V3_3ATA_N1 page 24: CN7 modify pin define page 25: modify FAN PWR control circuit
	304	page 16: ADD U23J99 PTP_PWR_ENH not for Touch pad PWR control page 25: ADD Touch pad control circuit
	302	page 18: modify HP_L / HP_R circuit
	304	page 09: U20J5 pin PWR well from +V3_3S page 16: Del S2_S2C / I2C_S2A not page 25: modify ELB control signal from EC to PCH
	308	page 21: change CN8 footprint page 25: modify ELB control signal from EC to PCH & change CN7 footprint page 22: change CN13 & CN10 footprint
	301	page 16: Del R533J83M4 page 27: change F12 footprint
	304	page 25: CN12 modify define
	C	
	407	page 26: Change CN4,CN5 footprint for SMT open issue
	402	page 25: Change Q25 PWR well to +V3_3 for electric leakage page 25: add R79AJ870J870AJC54,Q54,Q55 for touch pad Discharge
	D	
	609	page 16: add AC_protection function for charger and EC
	600	page 24: Del R170J816J816J822 for SMT open issue
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